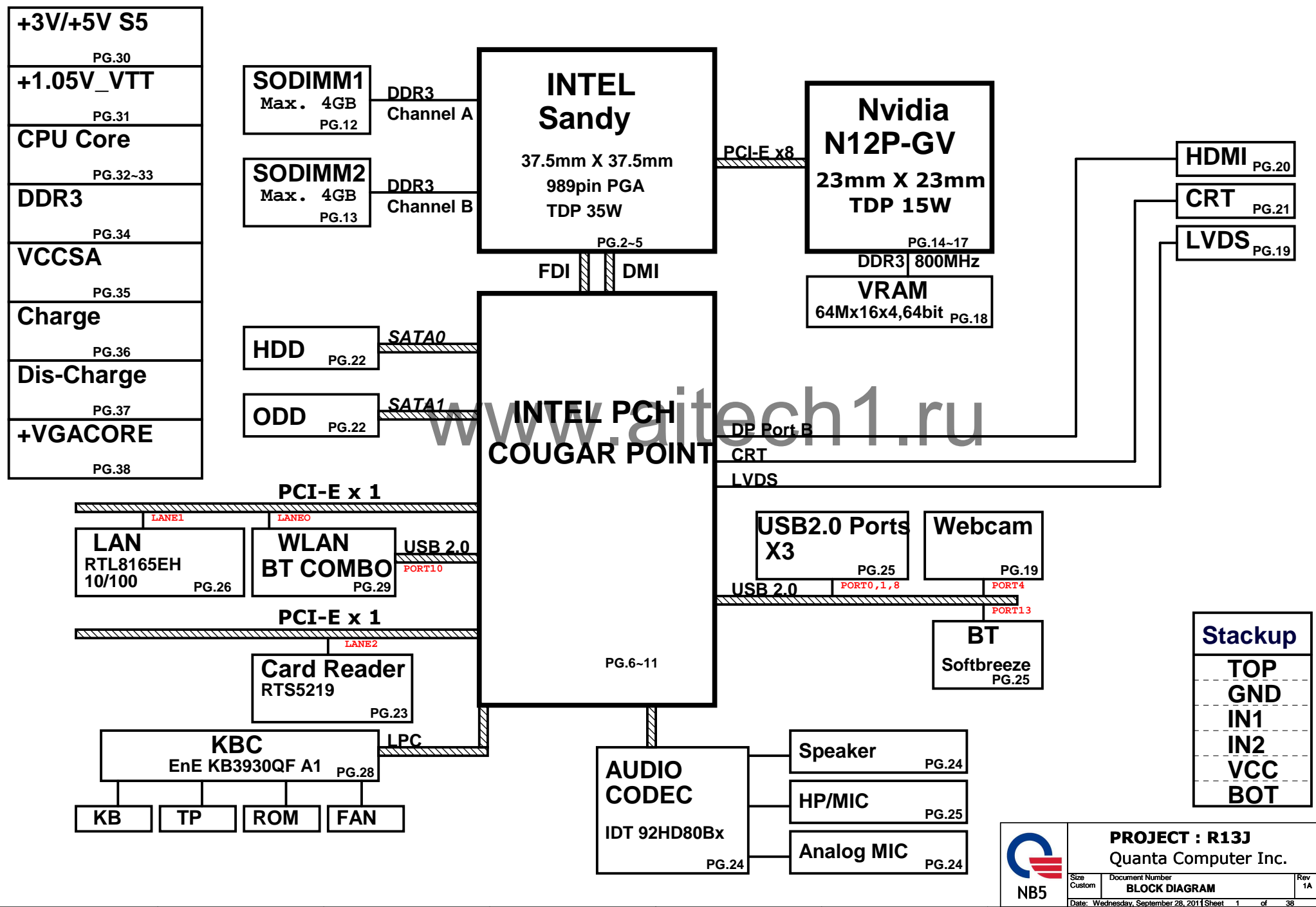
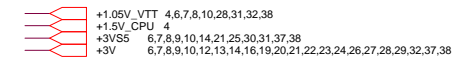


R13J INTEL UMA/DISCRETE SYSTEM DIAGRAM

01



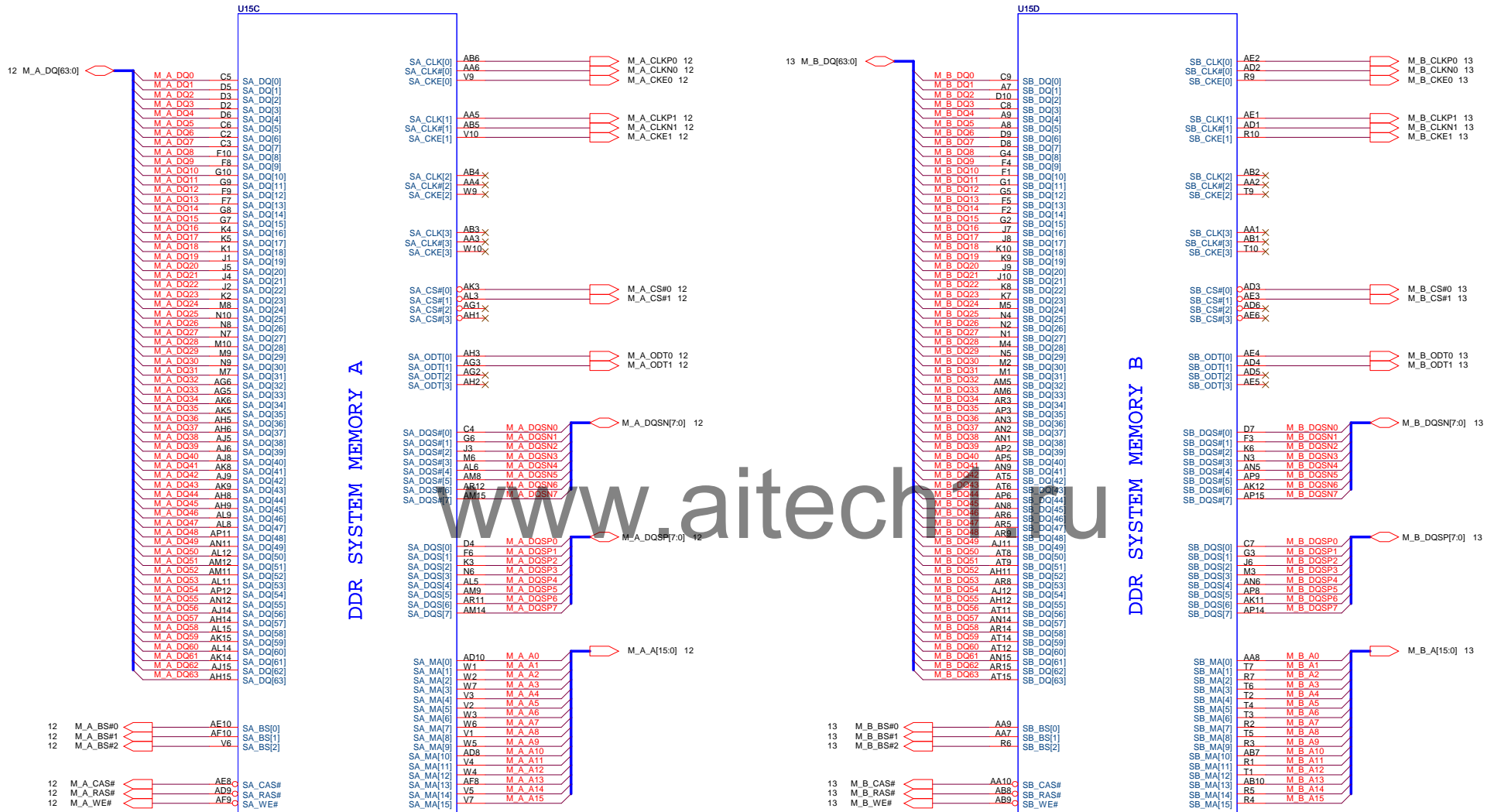


PROJECT : R13J

Quanta Computer Inc.

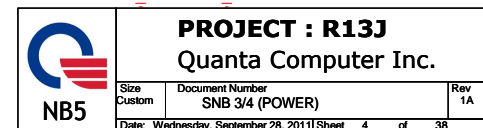
Size Custom	Document Number SNB 1/4 (PCIE&DMI&FDI)	Rev 1A
Date: Wednesday, September 28, 2011 Sheet 2 of 38		

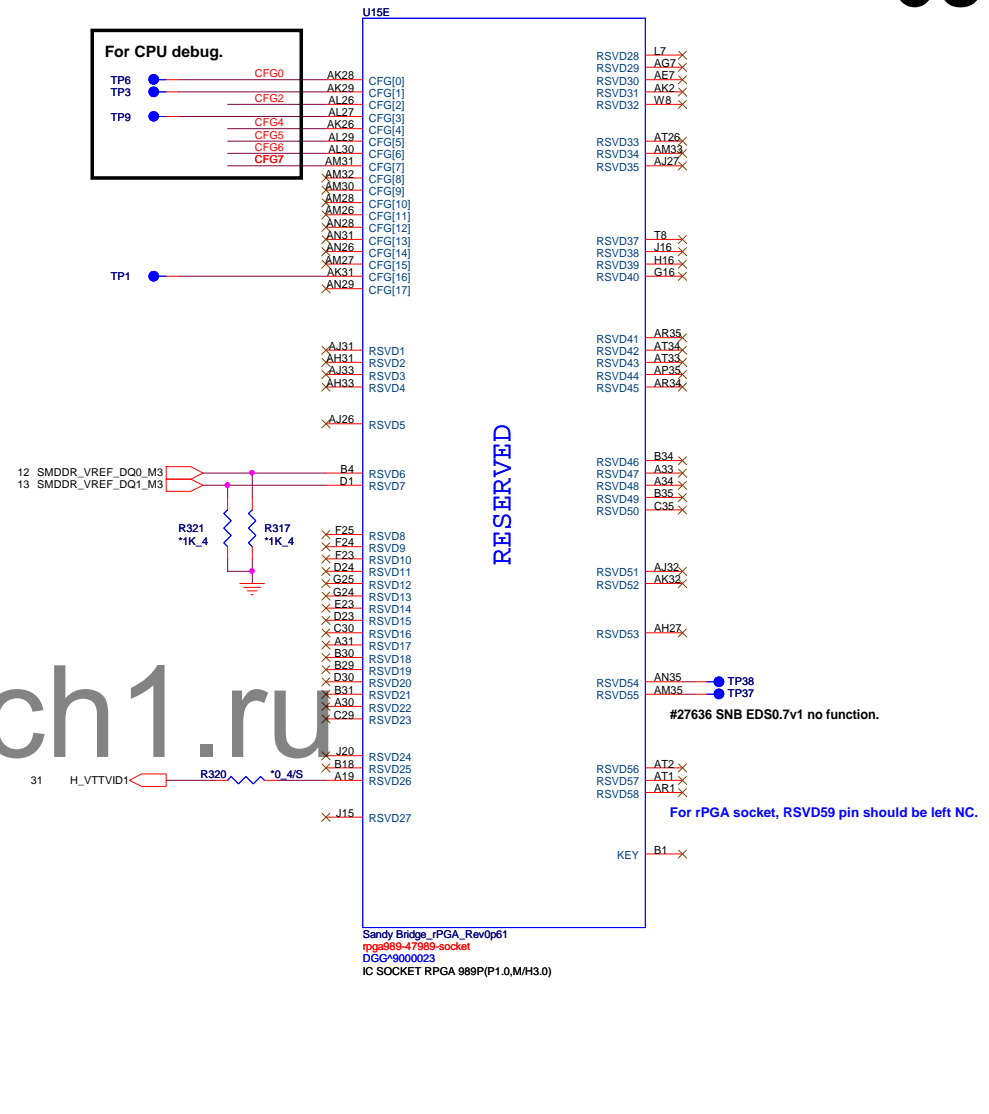
Sandy Bridge Processor (DDR3)



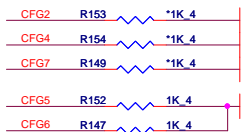
Sandy Bridge_rPGA_Rev0p61
rpg989-47989-socket
DGG-9000023
IC SOCKET RPGA 989P(P1.0,M/H3.0)

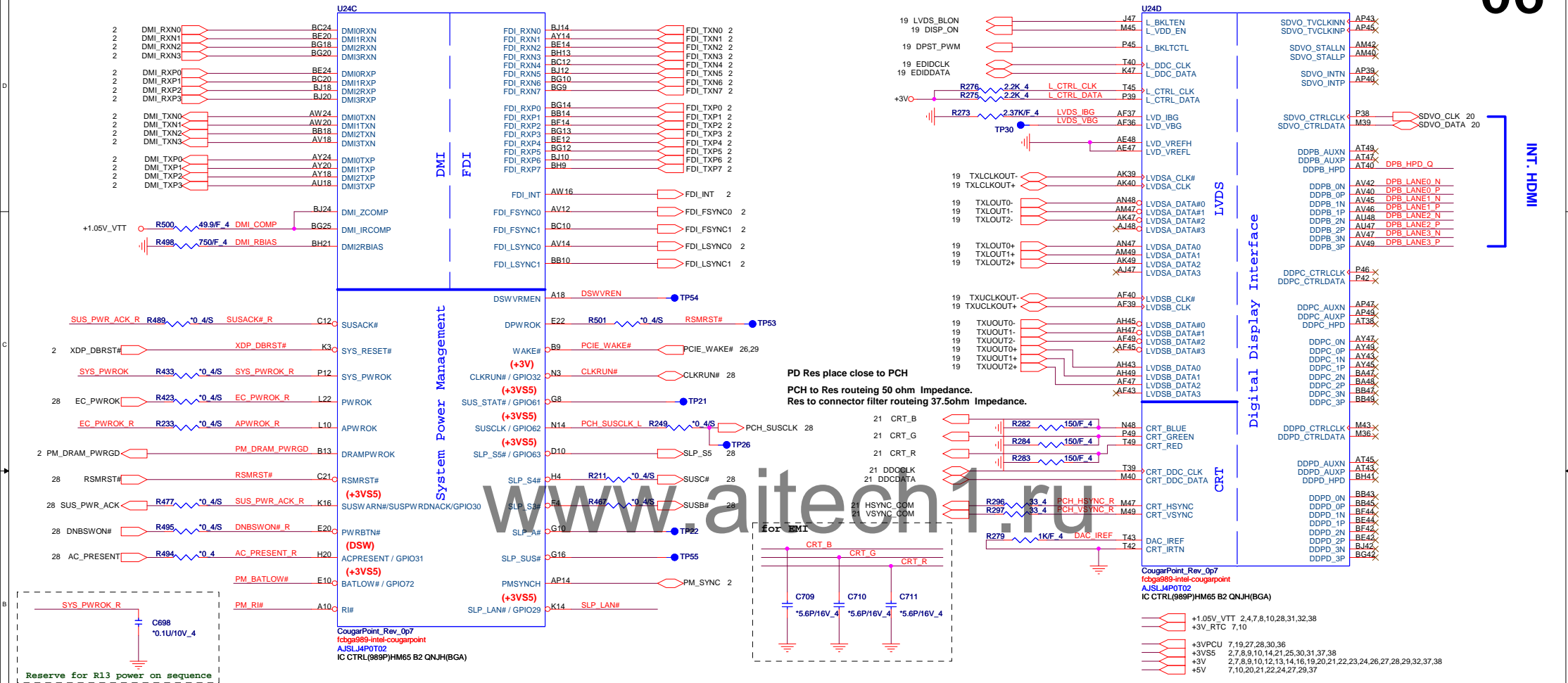
Sandy Bridge_rPGA_Rev0p61
rpg989-47989-socket
DGG-9000023
IC SOCKET RPGA 989P(P1.0,M/H3.0)



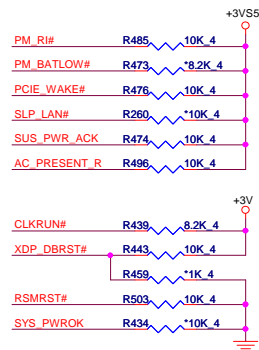


```
CFG[6:5] (PCIe Port Bifurcation Straps)
11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled
```

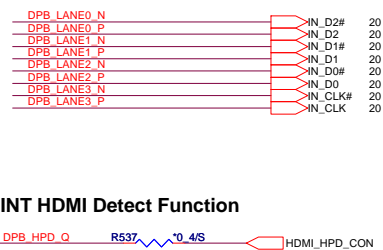




PCH Pull-high/low(CLG)



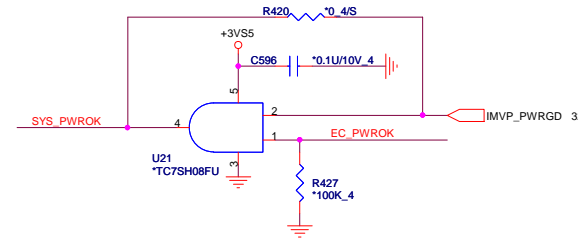
INT HDMI disable (DIS only remove)



INT HDMI Detect Function



System PWR_OK(CLG)



On Die DSW VR Enable

High = Enable (Default)

Low = Disable

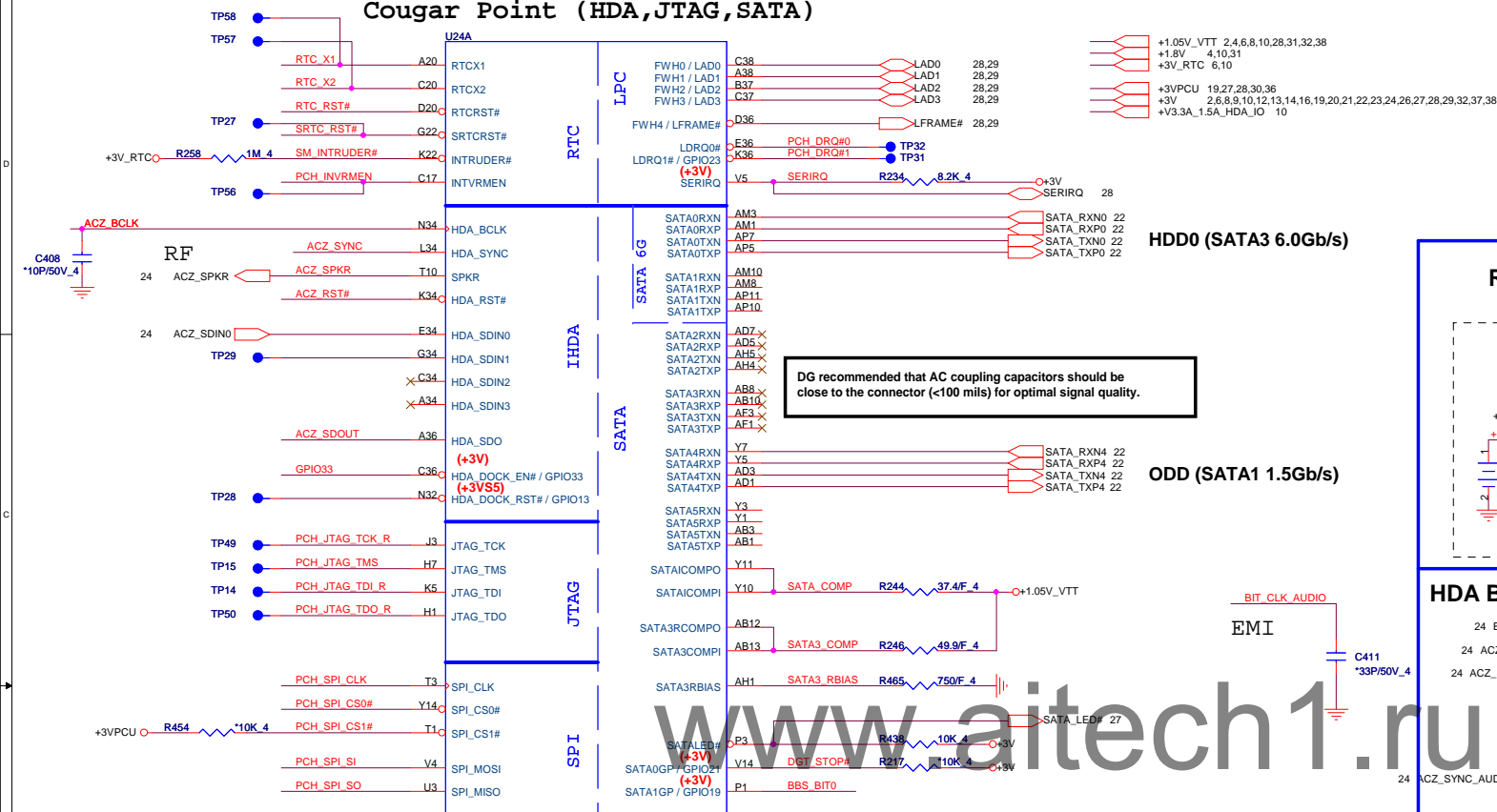


PROJECT : R13J

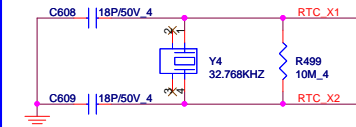
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 1/6 (DMI/FDI/VIDEO)	1A
Date:	Wednesday, September 28, 2011	Sheet 6 of 38

Cougar Point (HDA,JTAG,SATA)



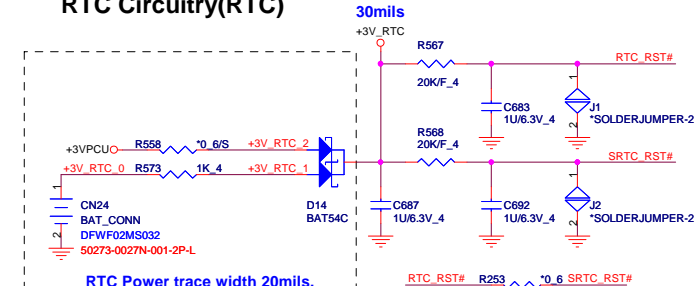
RTC Clock 32.768KHz



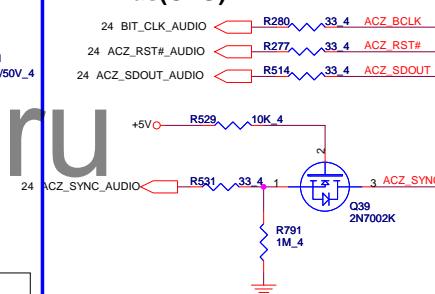
HDD0 (SATA3 6.0Gb/s)

ODD (SATA1 1.5Gb/s)

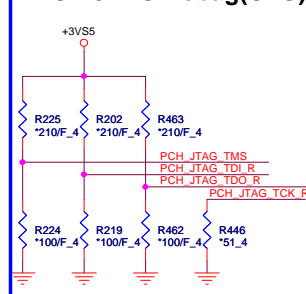
RTC Circuitry(RTC)



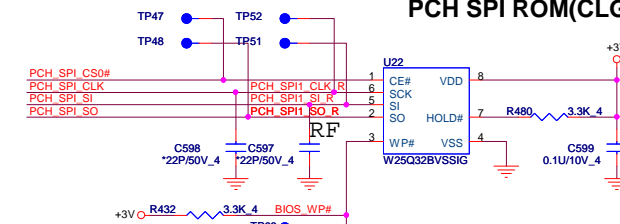
HDA Bus(CLG)



PCH JTAG Debug(CLG)



PCH SPI ROM(CLG)



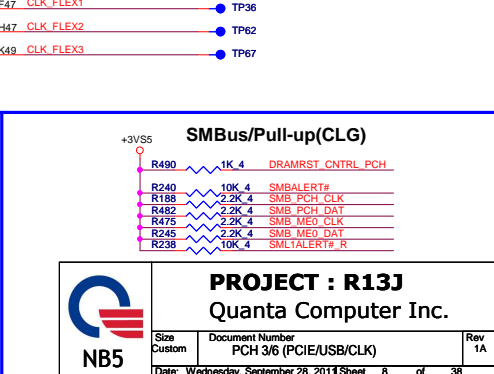
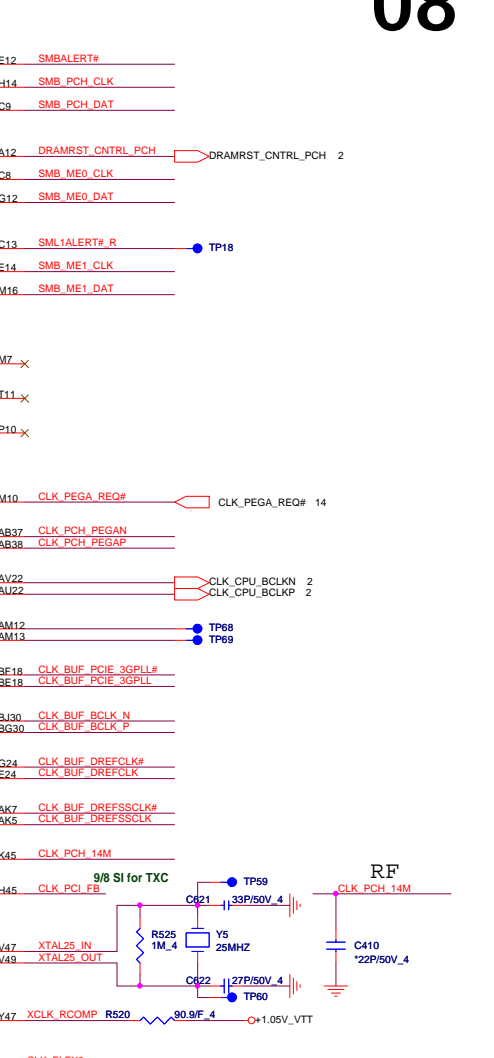
Vender	Size	P/N
EON	4MB	AKE39FN0Q00 (EN25F32-100HIP)
Winbond	4MB	AKE391P0N00 (W25Q32BVSSIG)
Socket		DG008000031

PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR	Different from Calpella No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	ACZ_SPKR R435 *1K 4 +3V
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R522 *1K 4 R521 10K 4 +3V PCI_GNT3# 8
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	PCH_INVRMEN R497 330K 4 +3V_RTC
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)	GPIO33 R509 0 4 BIOS_WP#
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	[Need external pull-down for LPC BIOS] Default weak pull-up on GNT0/1#	R455 *1K 4 BBS_BIT0
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK		R523 *1K 4 BBS_BIT1 8
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)	+1.8V R468 *1K 4 NV_ALE 8
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 20kohm	+1.8V R470 2.2K 4 R469 4.7K 4 NV_CLE 8 H_SNB_IVB# 2
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3V5 R278 1K 4 ACZ_SYNC
HDA_SDO	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)	GPIO33_E ACZ_SDOUT R510 *1K 4 +V3.3A_1.5A_HDA_IO
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)	R483 *1K 4 ICC_EN# 9
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	R447 *1K 4 PLL_ODVR_EN 9
SPI_MOSI	ITPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	PCH_SPI_SI R198 1K 4 +3V

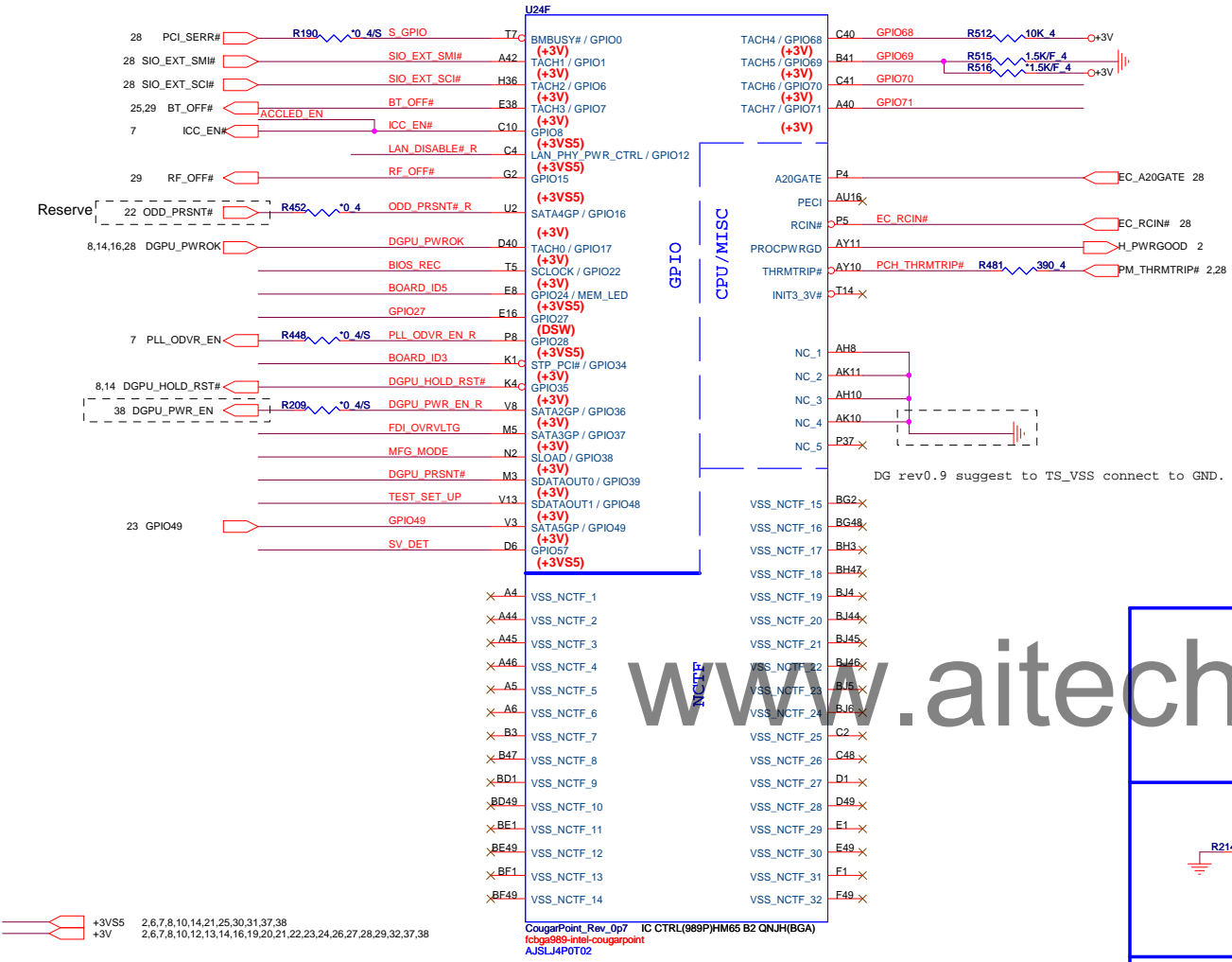
PROJECT : R13J
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 2/6 (SATA/HDA/SPI)	1A
Date:	Wednesday, September 28, 2011	Sheet 7 of 38

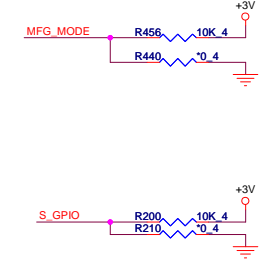


Cougar Point (GPIO,VSS_NCTF,RSVD)

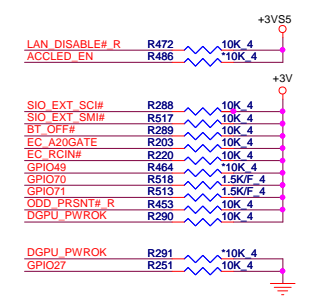
Clock Gen Power OK (CLG)



MFG-TEST



GPIO Pull-up/Pull-down(CLG)



RF_OFF# R449 1K 4 +3VSS5

Intel ME Crypto Transport Layer Security (TIS) cipher suite

Low = Disable (Default)

High = Enable

BIOS_REC R195 10K 4 +3V

BIOS RECOVERY High = Disable (Default) Low = Enable

TEST_SET_UP R196 10K 4 +3V

SV_SET_UP

High = Strong (Default)

SV_DET R235 10K 4 +3V

TEST DETECT

Low = Default

DGPU_PWR_EN_R R199 200K/F 4 +3V

DMI TERMINATION VOLTAGE OVERRIDE

Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

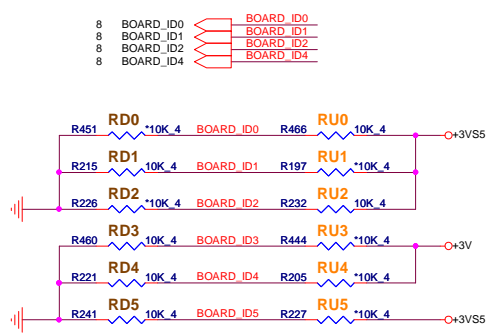
FDI_OVRVLGTG R218 1K 4 +3V

FDI TERMINATION VOLTAGE OVERRIDE

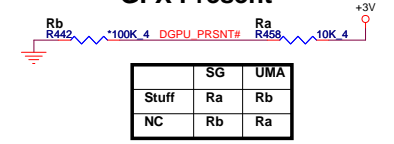
LOW - Tx, Rx terminated to same voltage

BOARD ID SETTING

Model	BOARD_ID5	BOARD_ID4	BOARD_ID3	BOARD_ID2	BOARD_ID1	BOARD_ID0
R13 UMA	0	0	0	0	0	0
R13 DIS	0	0	0	0	0	1
R13 (1.1) DIS (AMD)	0	0	0	0	1	1
R13J (1.3) DIS (NVIDIA)	0	0	0	1	0	1
	0	0	0	0	0	0



GFX Present



	SG	UMA
Stuff	Ra	Rb
NC	Rb	Ra

PROJECT : R13J

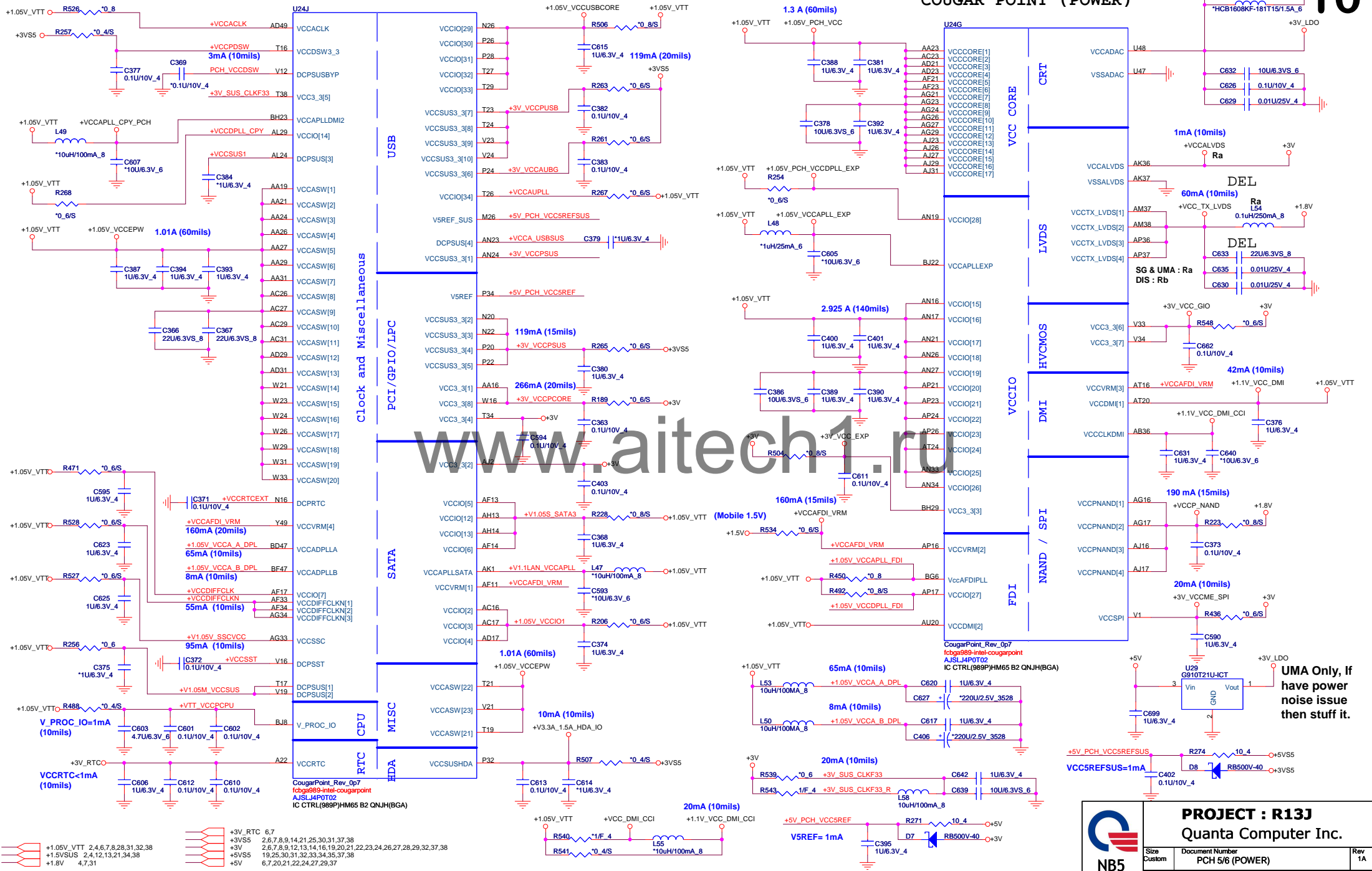
Quanta Computer Inc.

Size Custom	Document Number PCH 4/6 (GPIO/MISC)	Rev 1A
Date: Wednesday, September 28, 2011 Sheet 9 of 38		

Cougar Point-M (POWER)

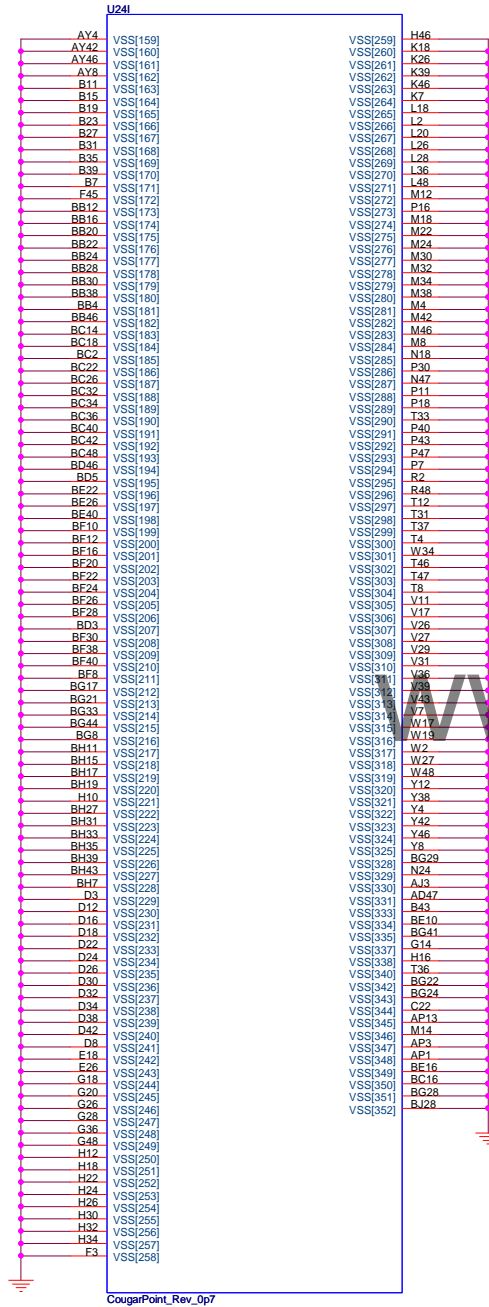
COUGAR POINT (POWER)

10

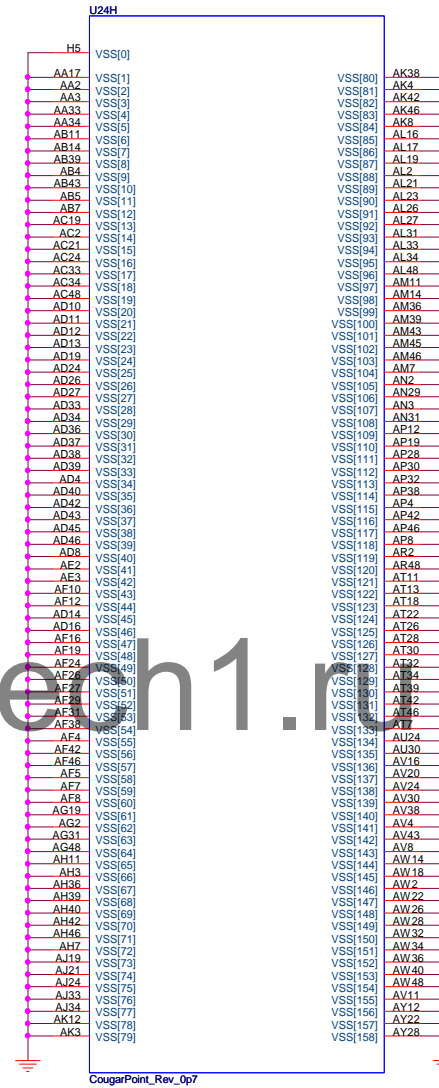


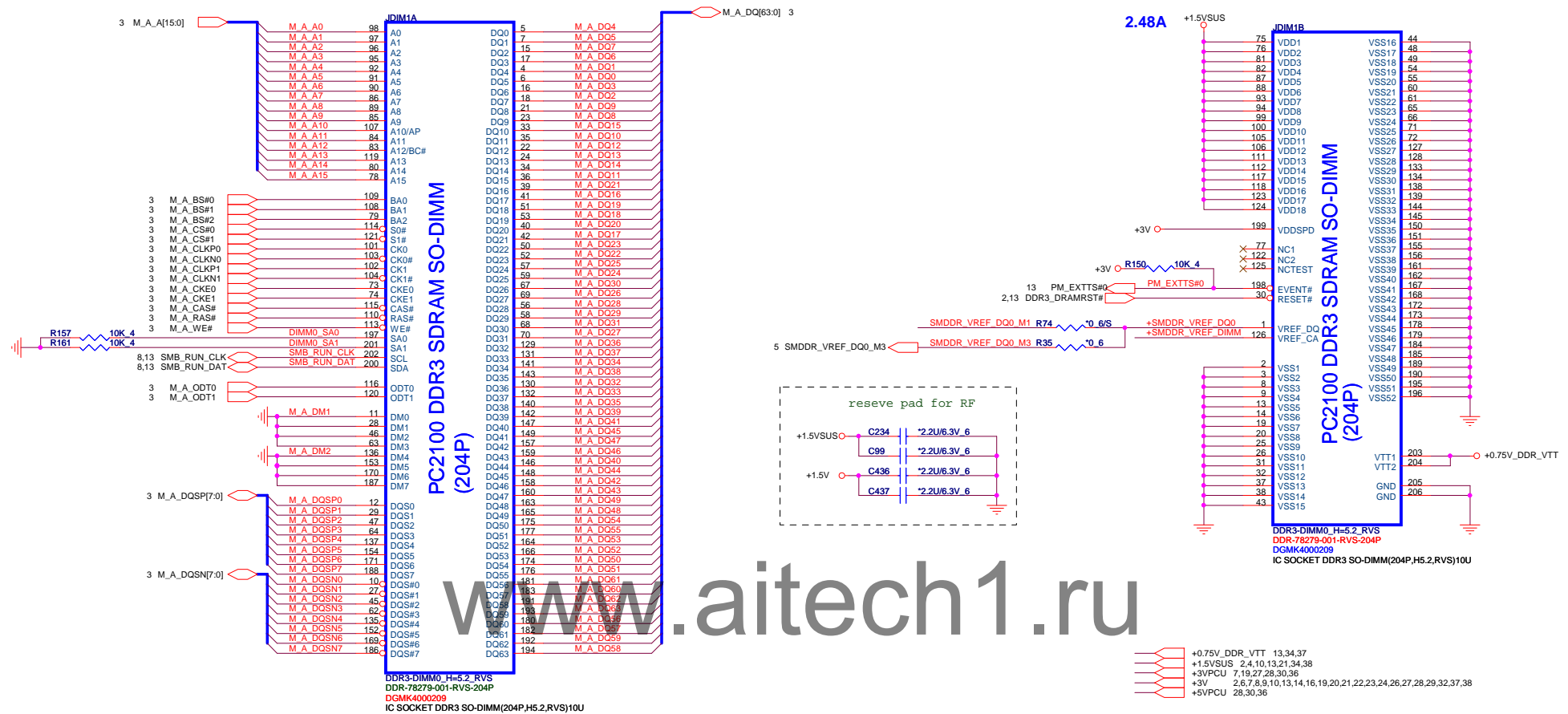
UMA Only, If have power noise issue then stuff it.

IBEX PEAK-M (GND)



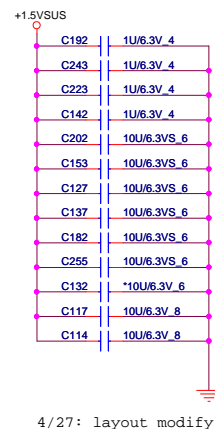
IBEX PEAK-M (GND)





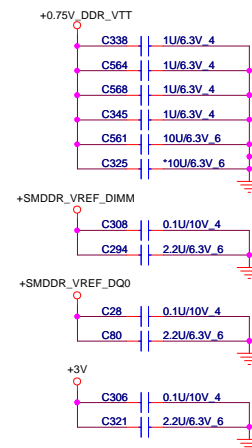
del M2 solution

VREF DQ0 M2 Solution

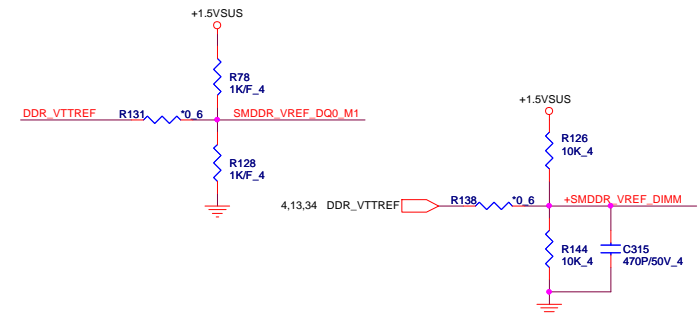


4/27: layout modify

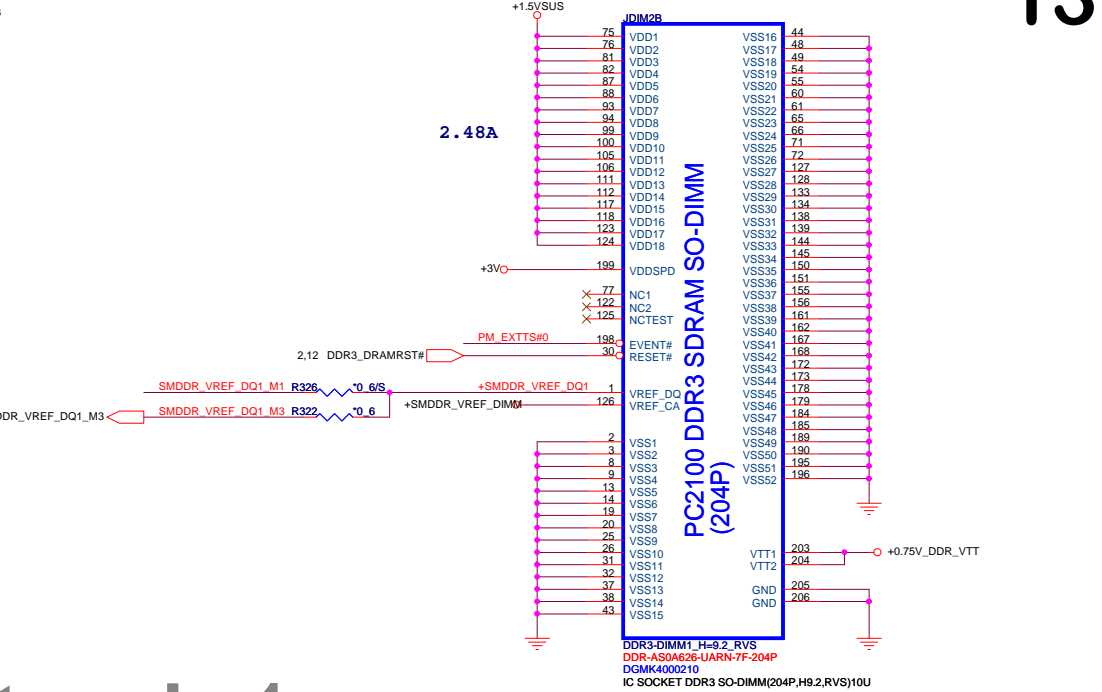
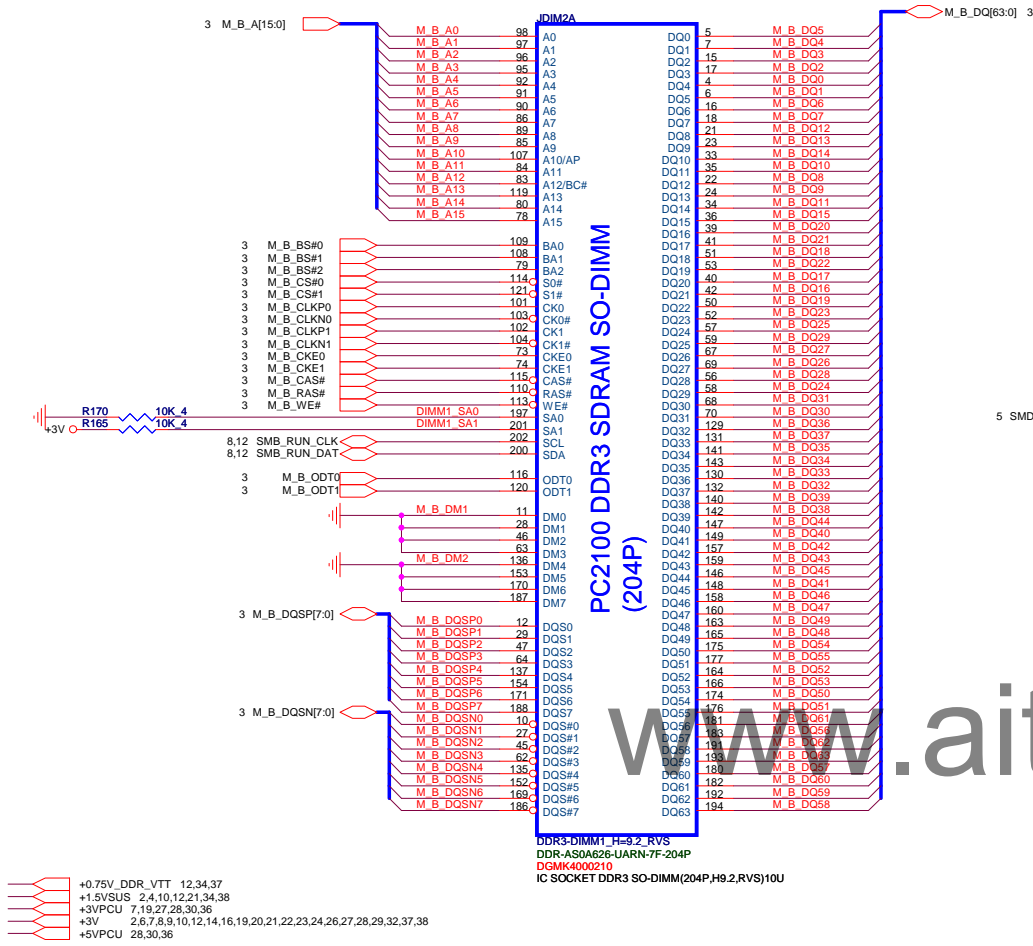
Place these Caps near So-Dimm0.



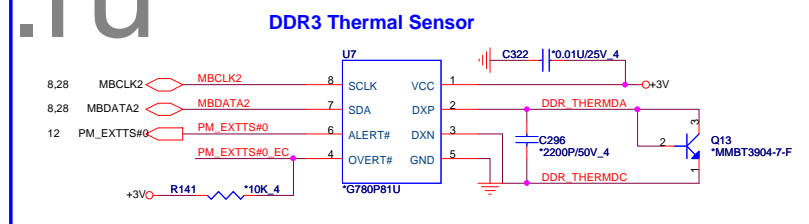
VREF DQ0 M1 Solution



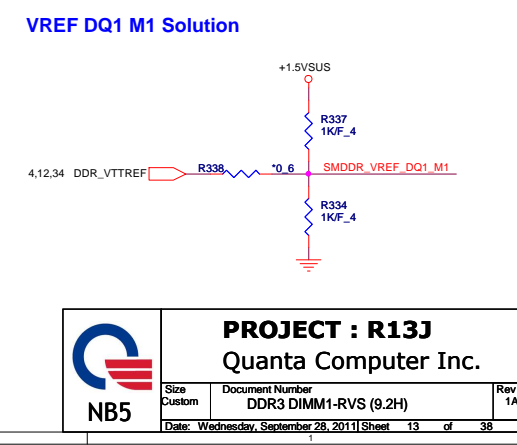
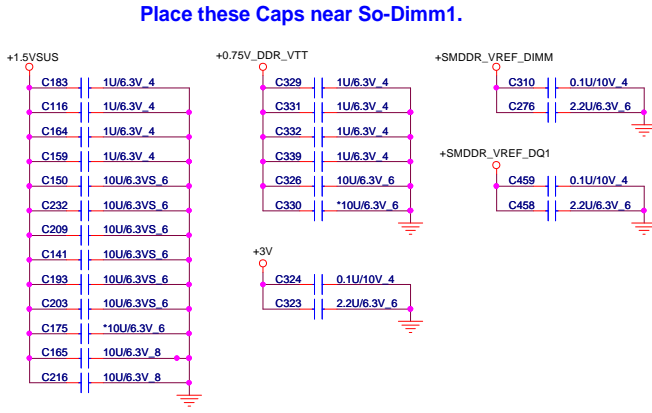
	PROJECT : R13J		
	Quanta Computer Inc.		
	Size Custom	Document Number DDR3 DIMM0-RVS (5.2H)	Rev 1A
Date: Wednesday, September 28, 2011 Sheet 12 of 38			



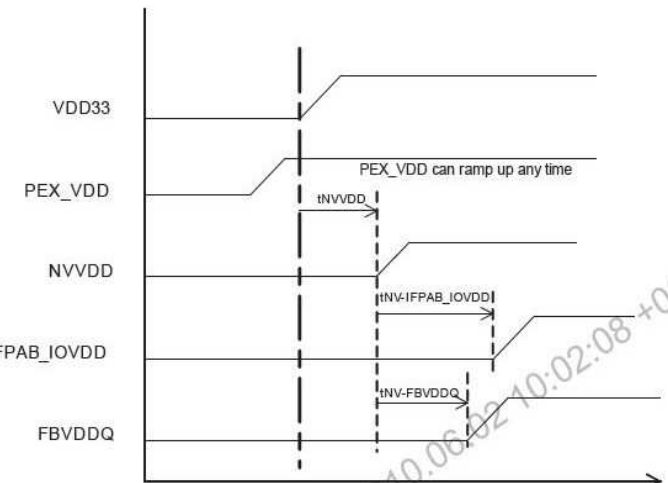
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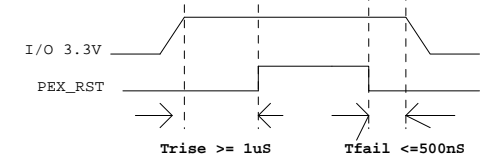
del M2 solution



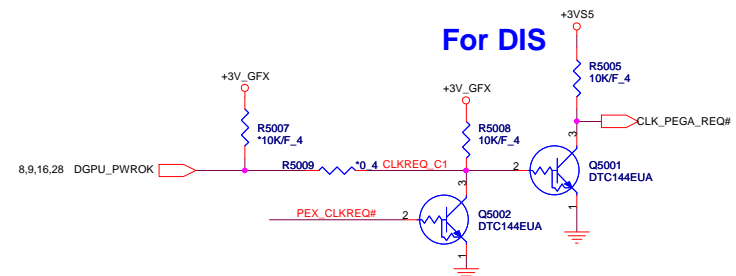
power up sequence



PEX_RST timing

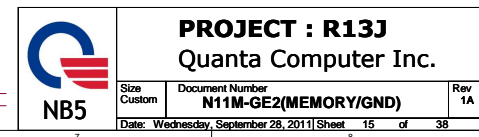


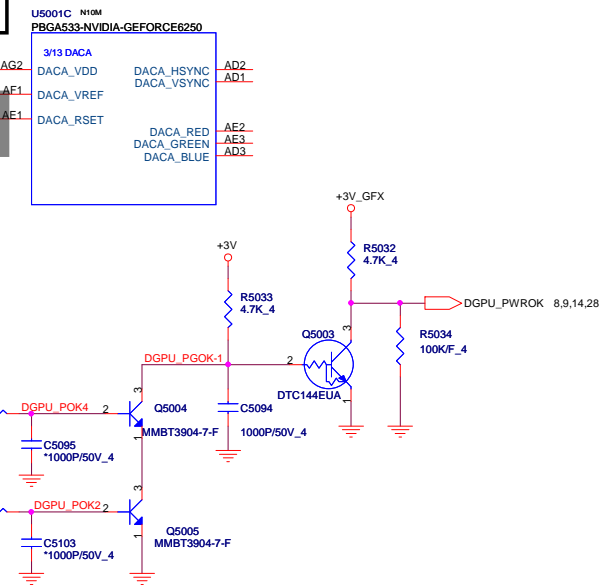
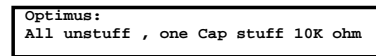
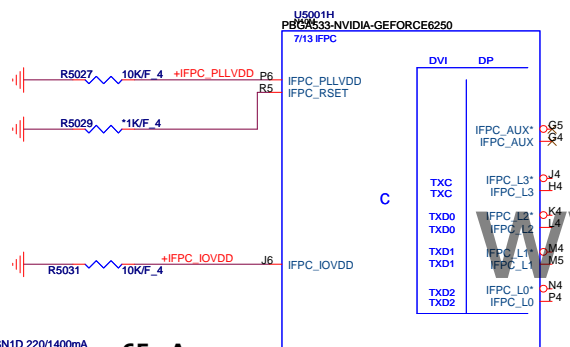
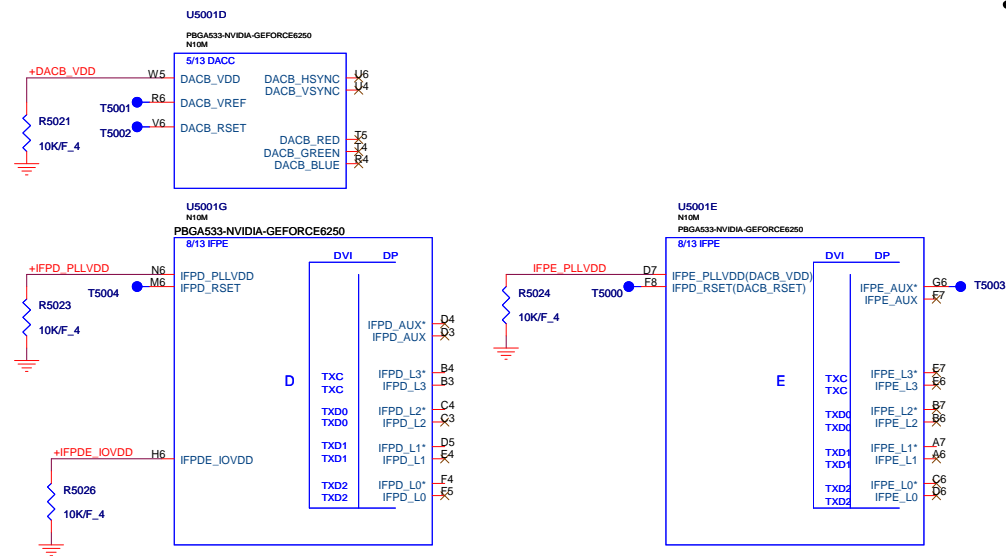
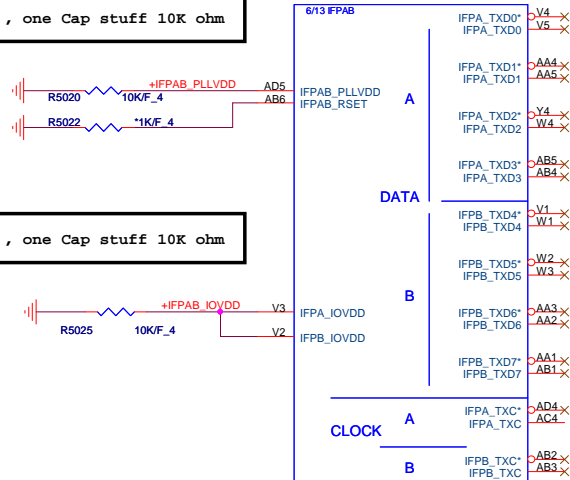
12/28 Nvidia to suggest R5009 not stuff and R5008 and Q5002 stuff.

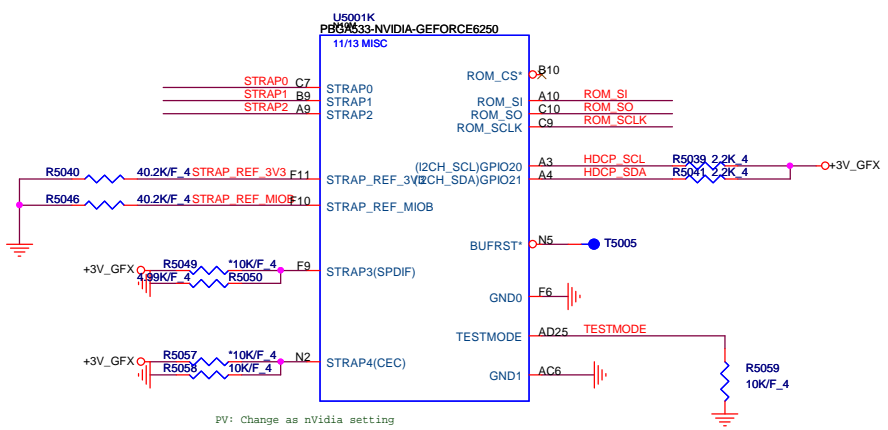


PROJECT : R13J
Quanta Computer Inc.

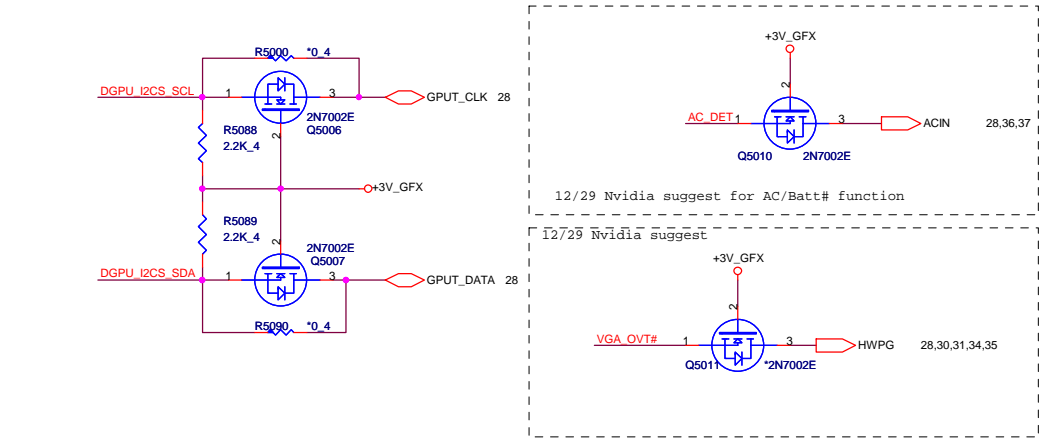
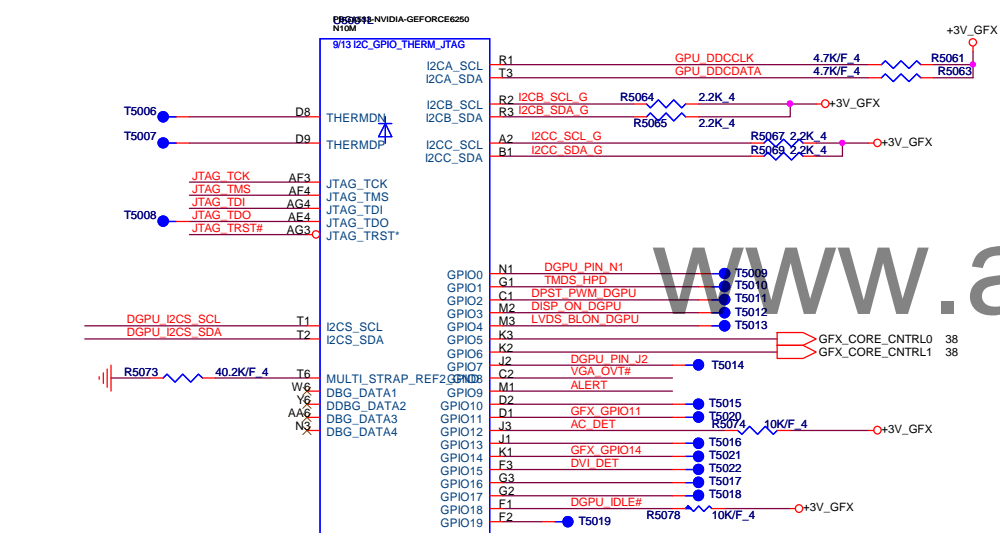
Size Custom Document Number N11M-GE2(PCIE/F) Rev 1A
Date: Wednesday, September 28, 2011 Sheet 14 of 38





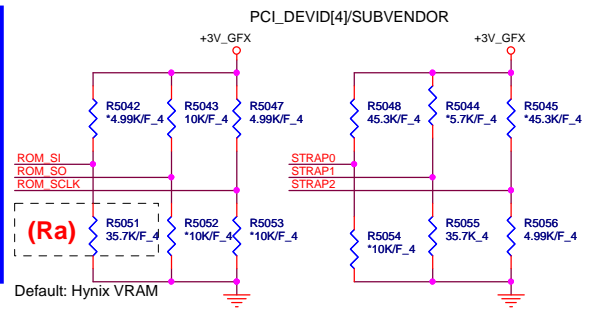


ROM_SI -> based on VRAM.
ROM_SO -> PU 10K
ROM_SCLK -> PU 5K
STRAP0 -> PU 45K
STRAP1 -> PD 35K
STRAP2 -> PD 5K
STRAP3 -> PD 5K
STRAP 4 -> PD 10K.



N12P-GV -> 0x17F
N12M-GE -> 0xA7A 1010 -> PU15K

Logical Strap Bit Mapping		
	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111




	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	PCI_DEVICE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	RESERVED	RESERVED	PCIE_MAX_SPEED	DP_PLL_VDD3V

RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	QCI P/N	ROM_SI
0000		Reserved			
0010	DDR3 64Mx16x8, 128bit, 1GB, 800MHz	Hynix			PD 15K
0011	DDR3 64Mx16x8, 128bit, 1GB, 800MHz	Samsung			PD 20K
0110	DDR3 128Mx16x4, 128bit, 1GB, 800MHz	Hynix	H5TQ2G63BFR-11C	AKD5MGWTW07	PD 35K
0111	DDR3 128Mx16x4, 128bit, 1GB, 800MHz	Samsung	K4W2G1646C-HC11	AKD5MGWT508	PD 45K
XXXX					

GPIO ASSIGNMENTS

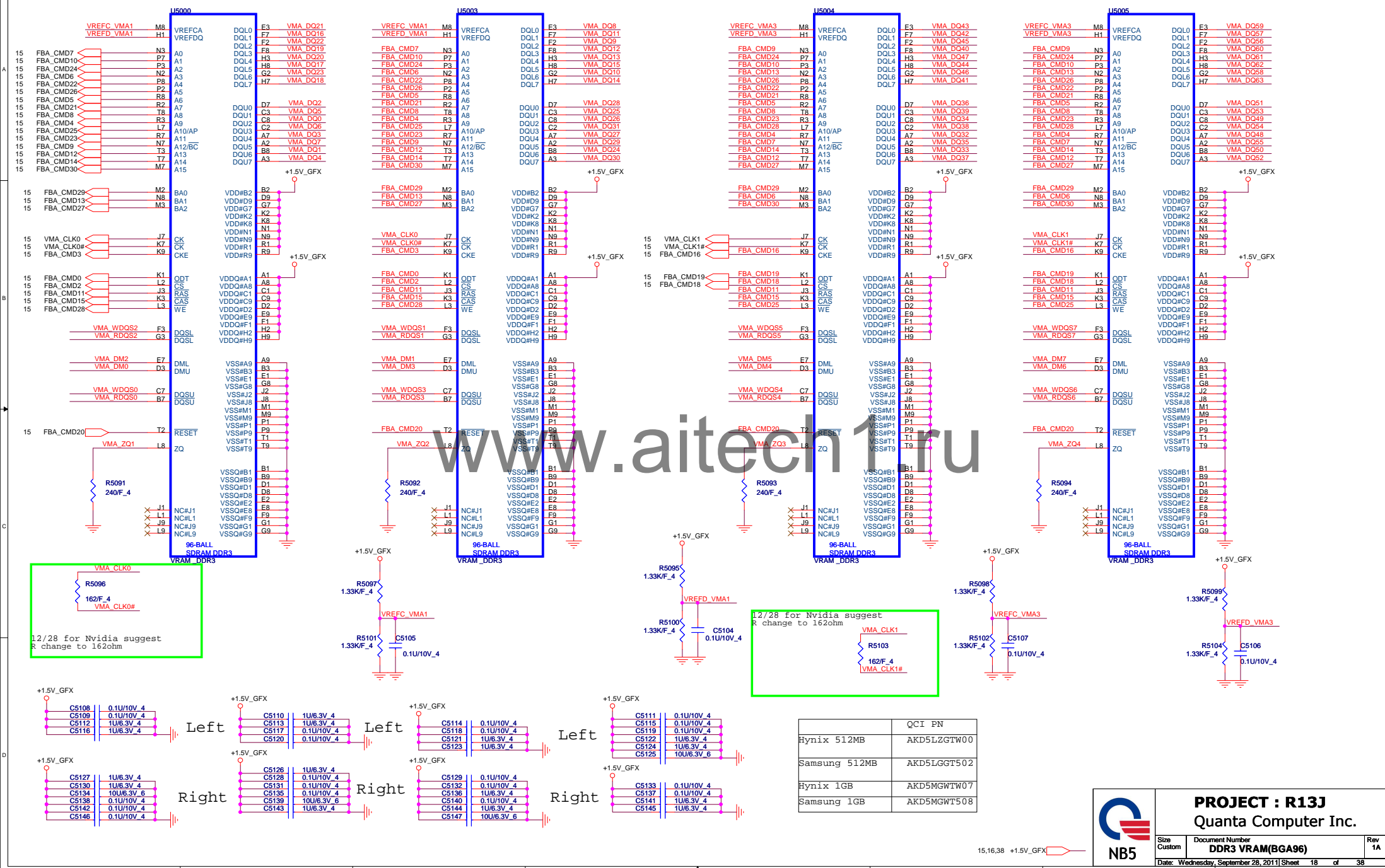
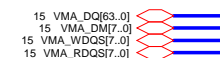
GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	I-C-T
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVD VDD0
6	OUT	N/A	NVVD VDD1
7	OUT	N/A	NVVD VDD2
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	Memory VREF SELECT
11	I/O	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL
13	OUT	N/A	THERM_LOAD_STEP_DOWN
14	OUT	N/A	THERM_LOAD_STEP_UP



PROJECT : R13J
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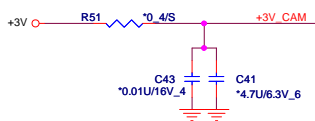
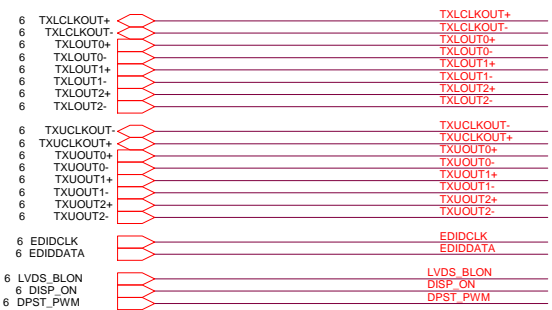
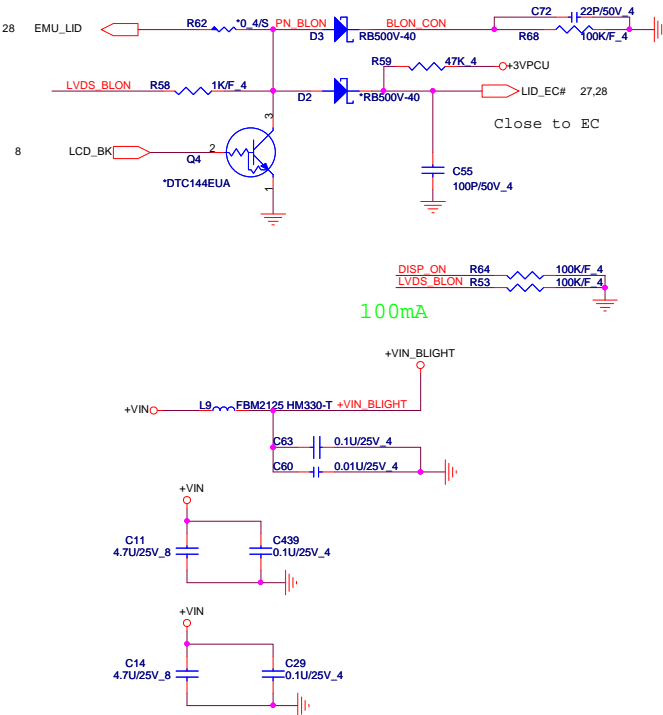
Size Custom	Document Number N12P-GV(GPIO/STRAPS)	Rev 1A
Date: Wednesday, September 28, 2011 Sheet 17 of 38		

CHANNEL A: 256MB/512MB DDR3



	QCI PN
Hynix 512MB	AKD5LZGTW0
Samsung 512MB	AKD5LGGT50
Hynix 1GB	AKD5MGWTW0
Samsung 1GB	AKD5MGWT50

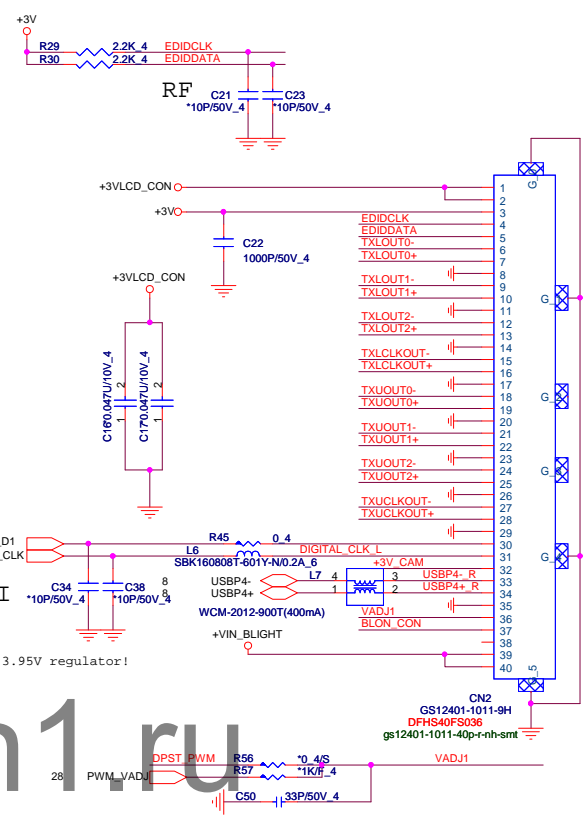
LID Switch



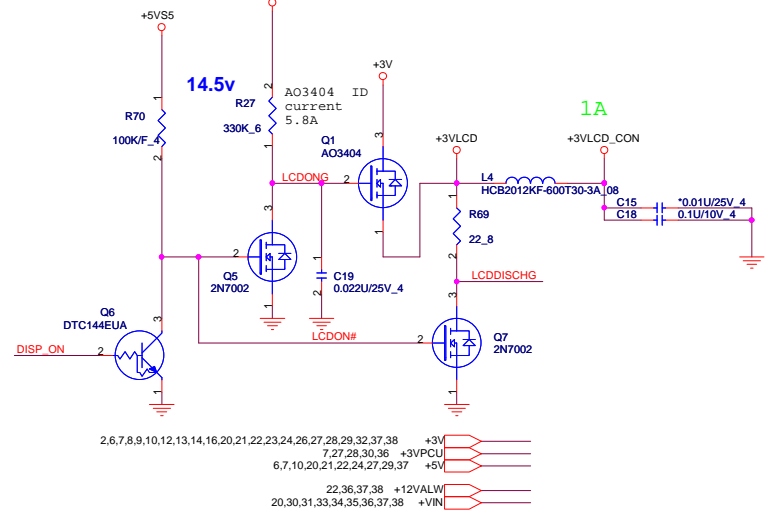
Please note that 2011 camera is +3V a We do not need to use 5V -> 3.95V regulator!

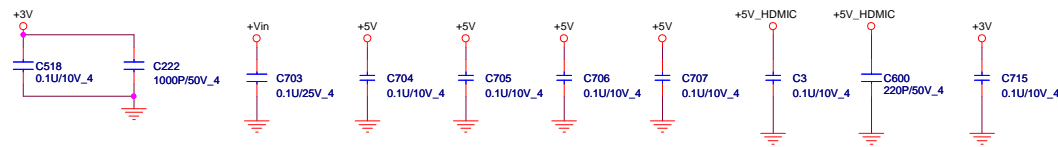
follow L7 location

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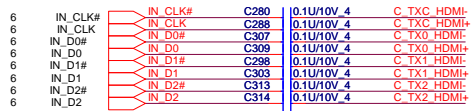


change to +5VS5

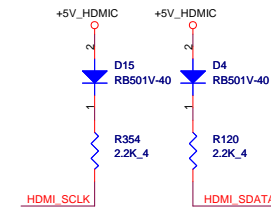
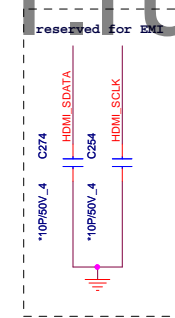
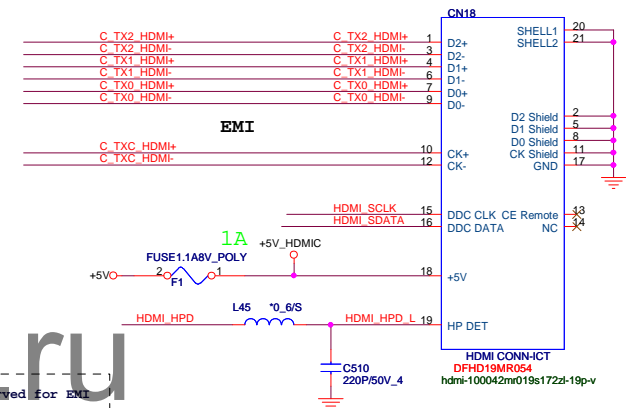
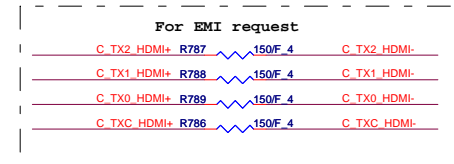
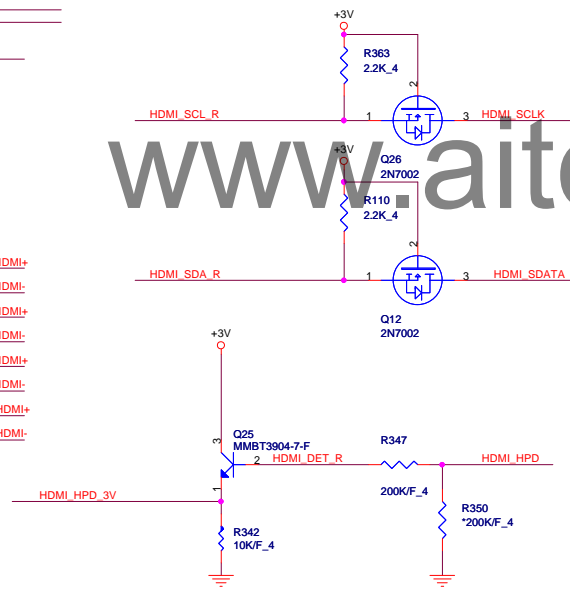
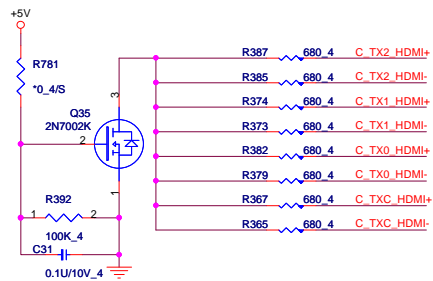


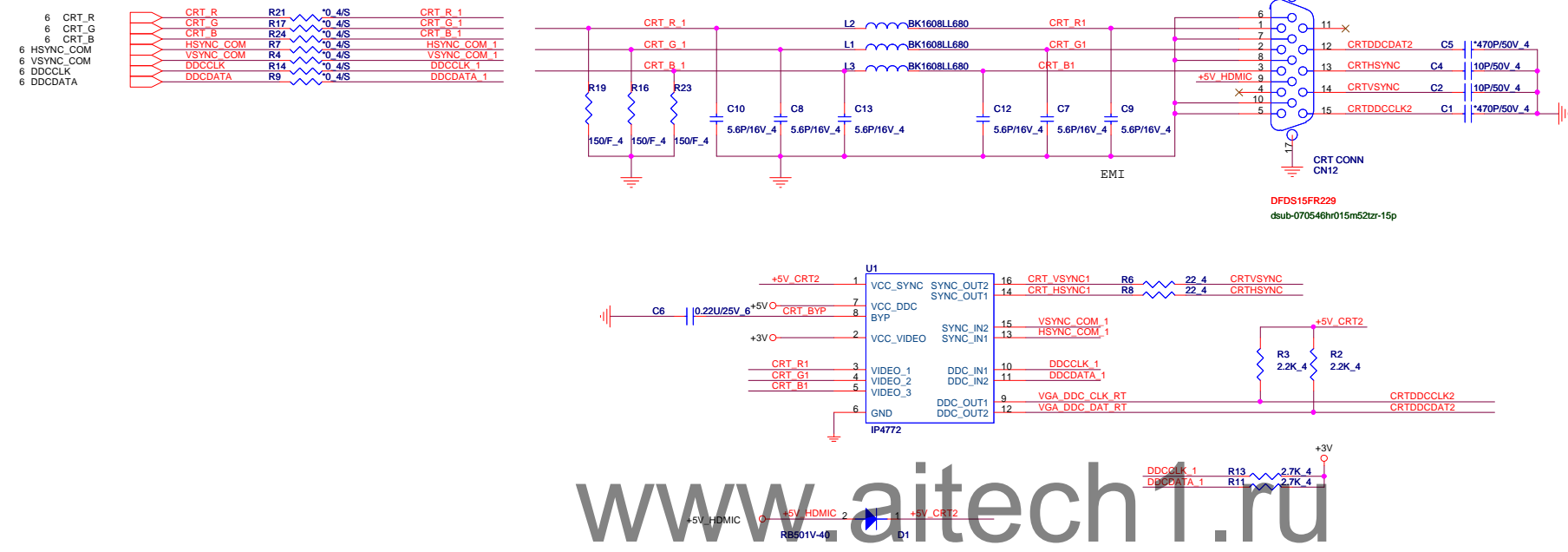


close to HDMI conn



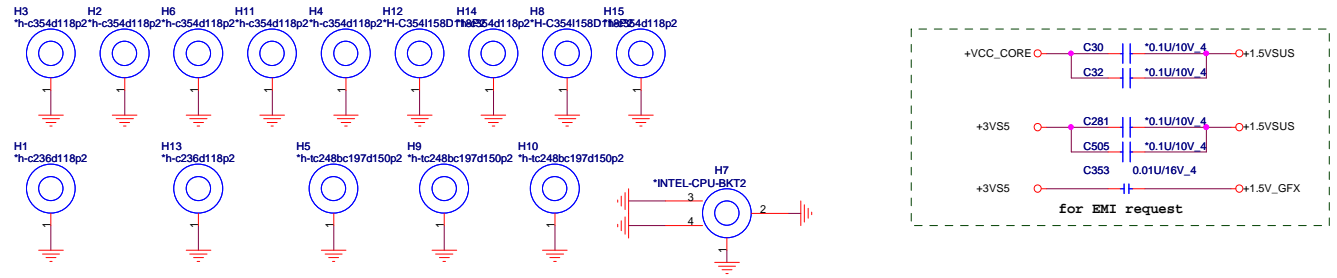
Close to HDMI Connector



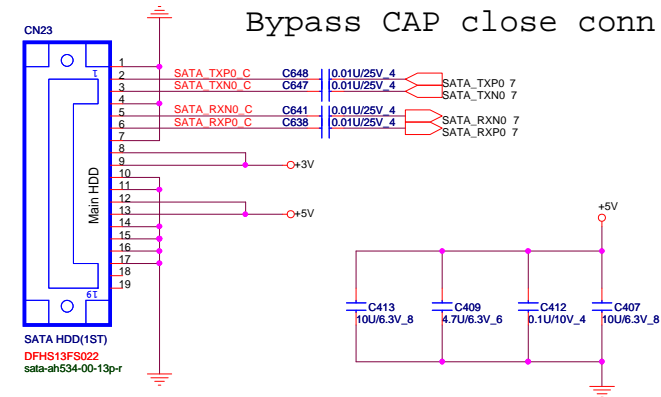


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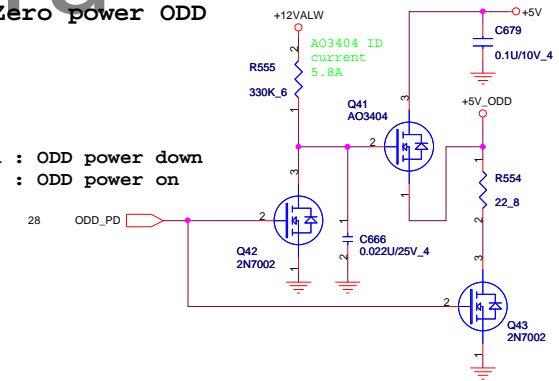
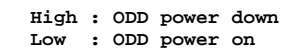
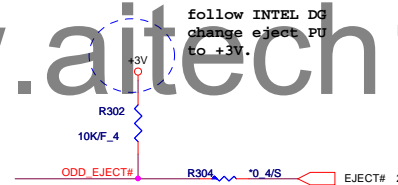
HOLE

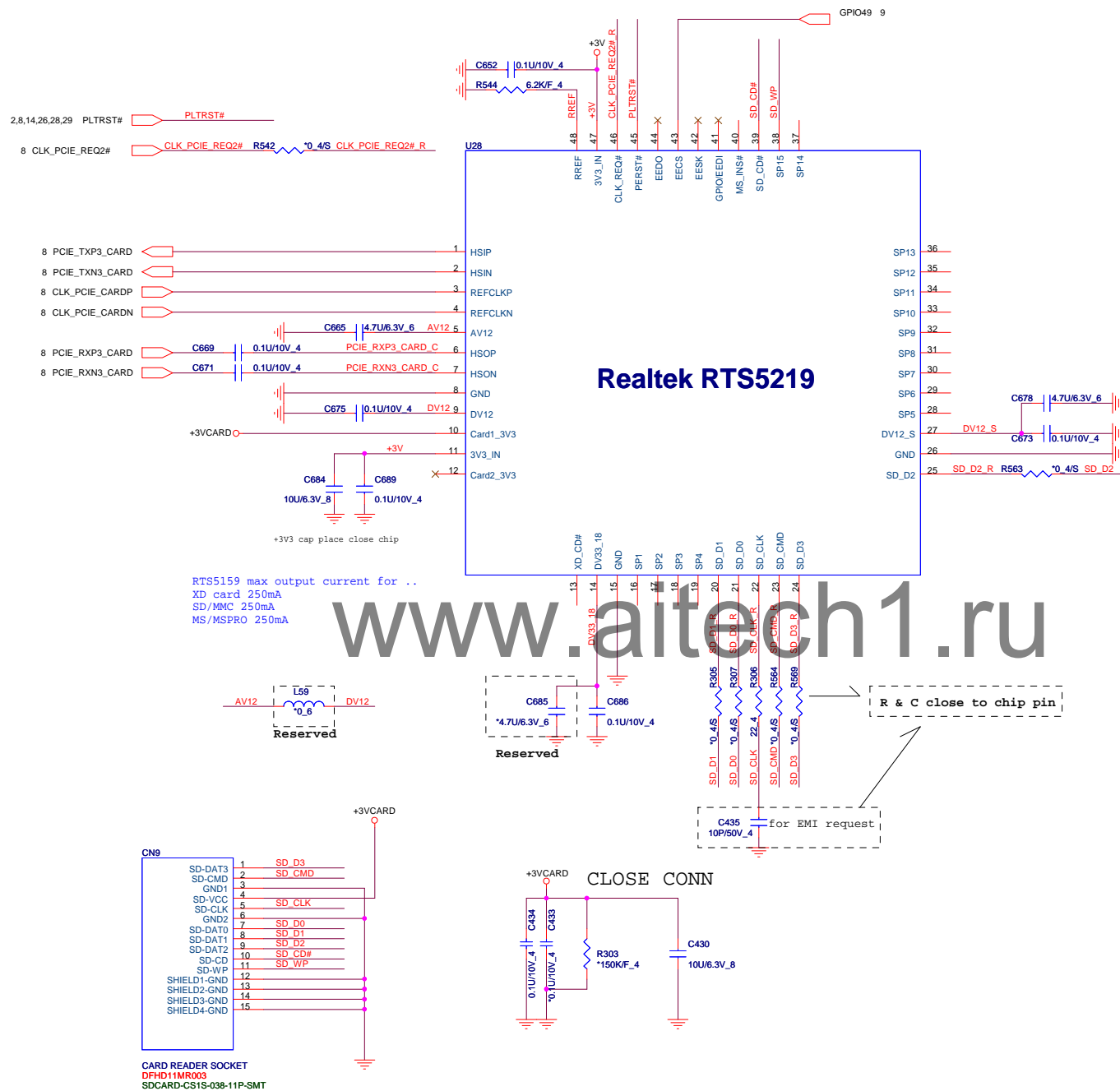


22

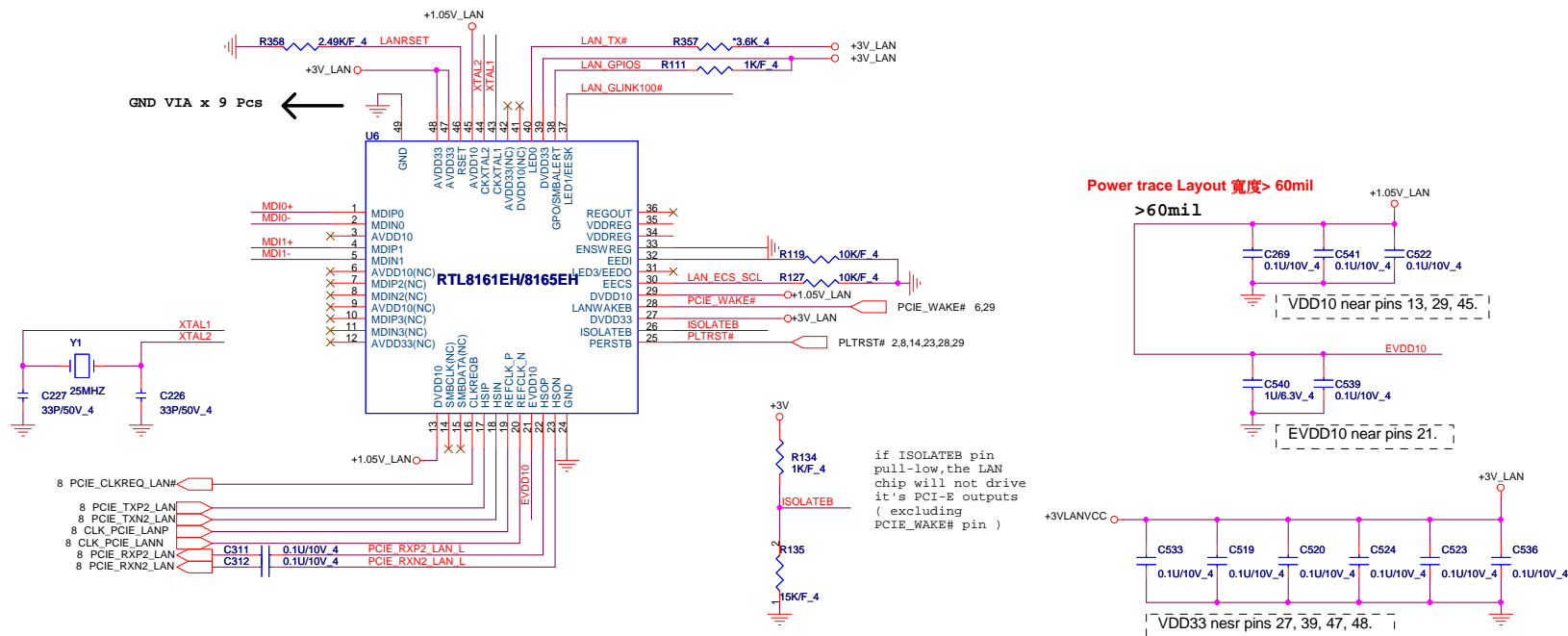


follow INTEL DG
change eject PU
to +3V.

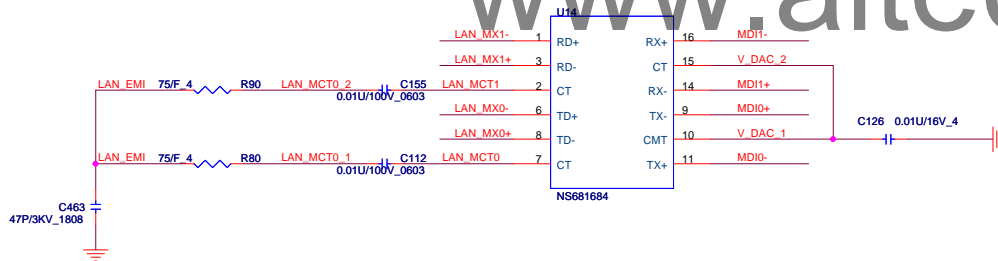




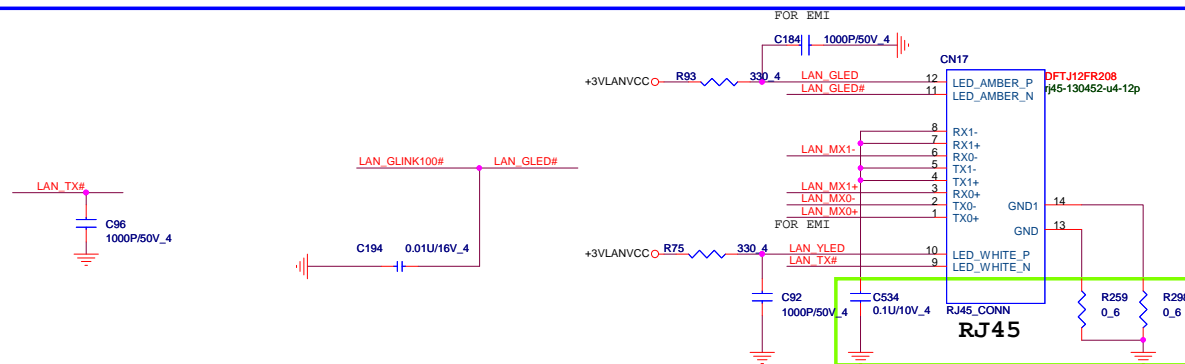




Transformer for 10/100



Lan Con.



2,6,7,8,9,10,12,13,14,16,19,20,21,22,23,24,27,28,29,32,37,38 +3V

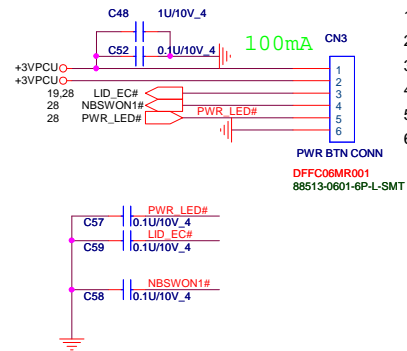


PROJECT : R13J
Quanta Computer Inc.

Size Custom	Document Number RTL8165EH	Rev 1A
Date: Wednesday, September 28, 2011 Sheet 26 of 38		

Reserved for ISN solution

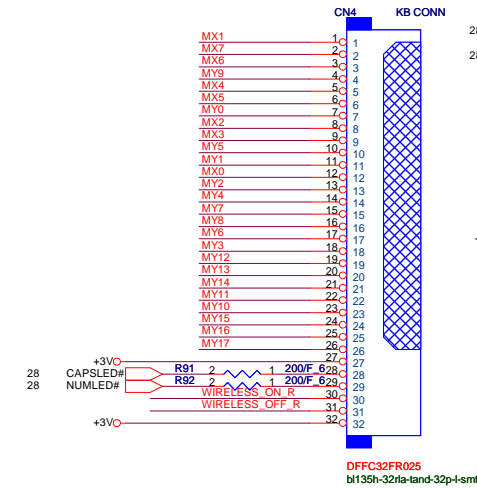
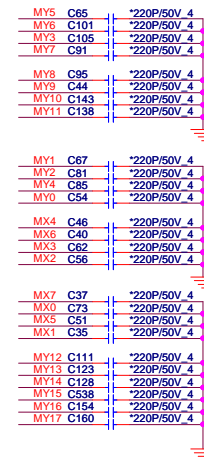
POWER BOTTON CONNECT



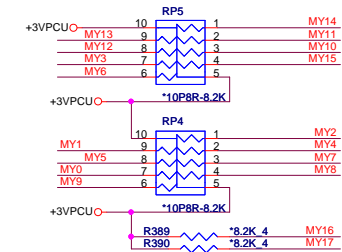
1. +3VPCU(LIDSWITCH PWR)
2. LEDVCC(+3VPCU)
3. LIDSWITCH
4. POWERON#
5. PWRLED#
6. GND

PWR_BTN_CONN
DFFC06MR001
88513-0601-6P-L-SMT

KEYBOARD Con.

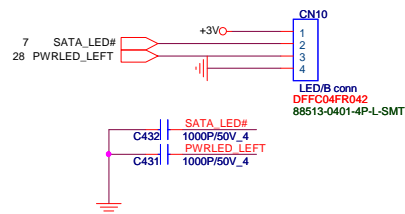


KEYBOARD PULL-UP

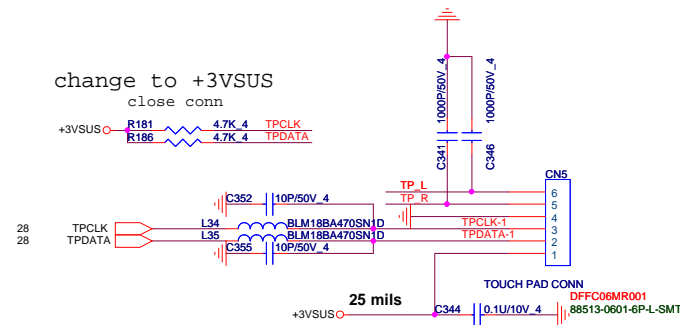


LED Con.

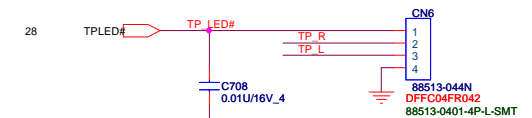
1. +3V
2. SATA_LED#
3. PWR_LED#
4. GND



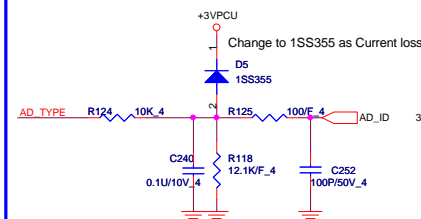
TOUCH PAD Con.



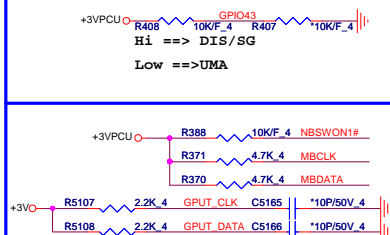
To TOUCH PAD SW board



adapter Type check

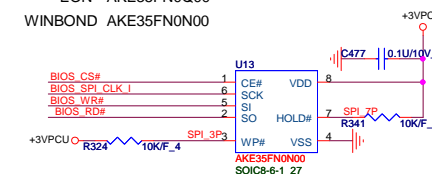


adapter select for EC

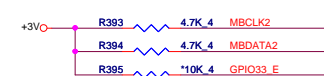


128K byte SPI EC ROM

Socket: DG008000031
EON AKE35FN0Q00
WINBOND AKE35FN0N00



INPUTS				OUTPUTS	
PRE	CLR	CLK	D	Q	\bar{Q}
L	H	X	X	H	L
H	H	X	X	L	H
L	H	X	X	H	L
H	H	X	X	L	H
H	H	-	H	H	L
H	H	-	L	L	H
H	H	L	X	Q ₀	\bar{Q}_0



Change to RB500 as Current loss

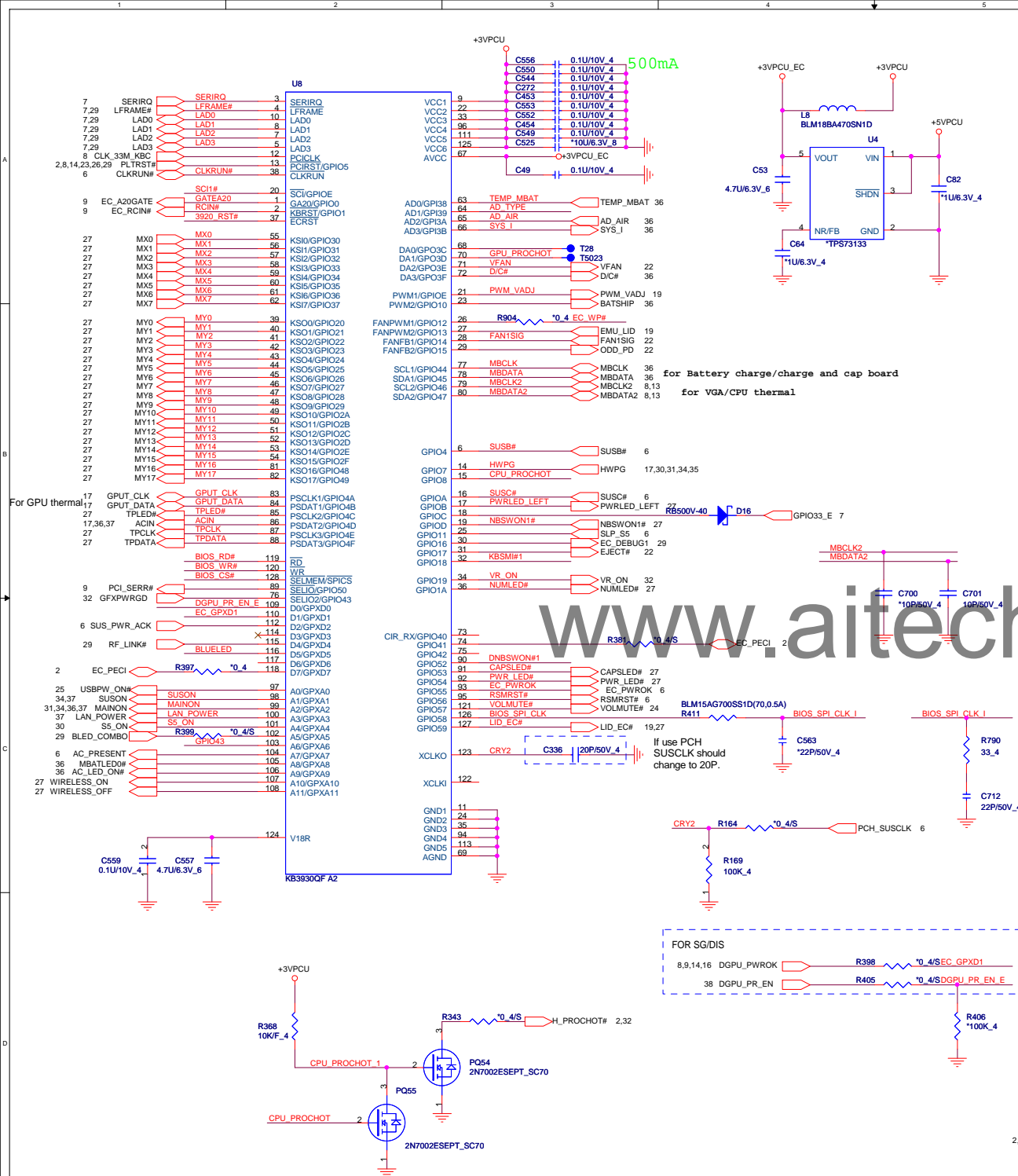
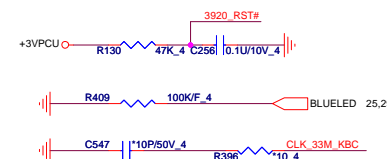
SCI1# D9 1 2 RB501V-40 SIO_EXT_SCI# 9

DNBSWON#1 D10 1 2 RB500V-40 DNBSWON# 6

KBSMI#1 D6 1 2 RB500V-40 SIO_EXT_SMI# 9

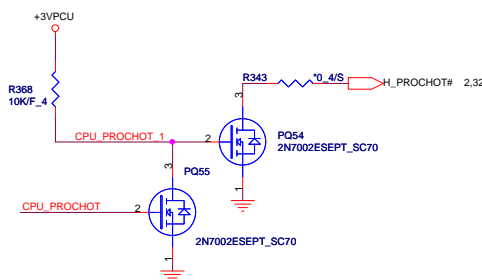
Add Pin 117,103 for DSM,116 for Bluetooth

Delete T10 and tie pin 117 from Lan for DSM



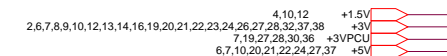
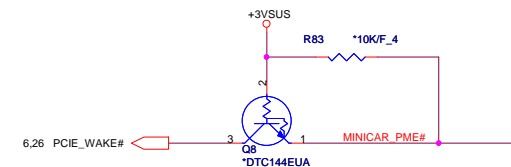
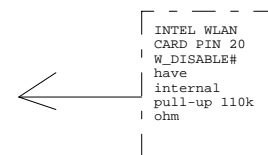
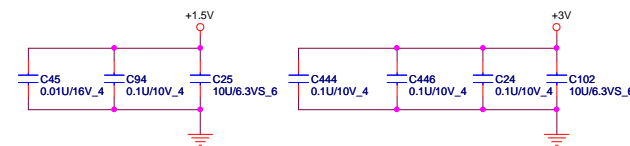
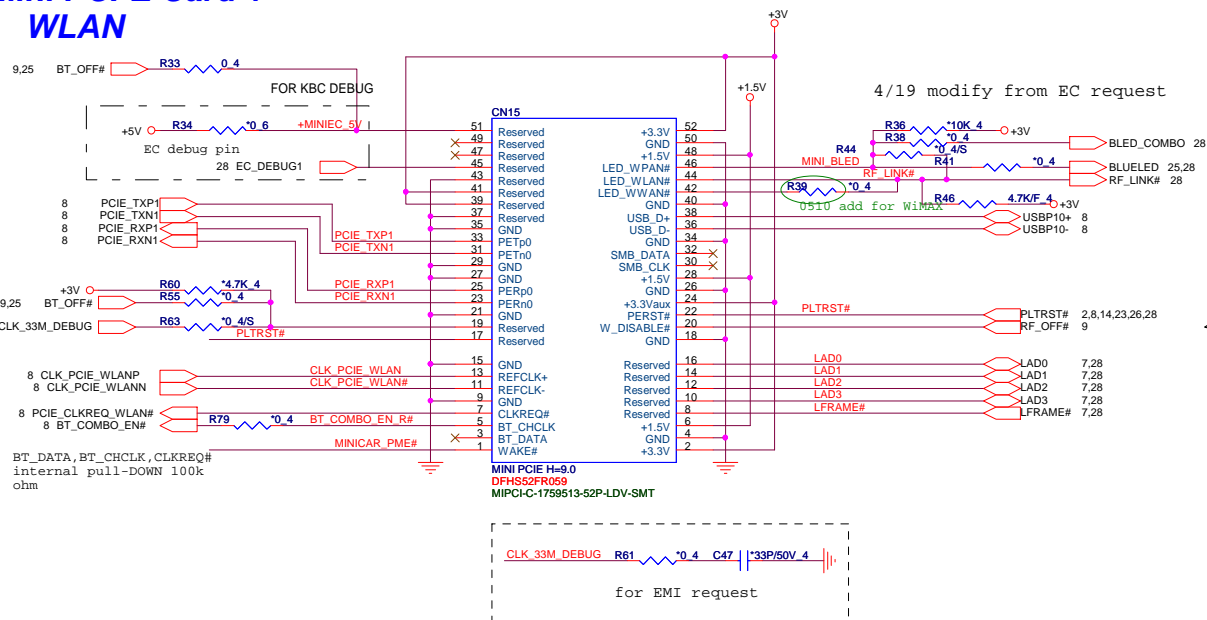
FOR SG/DIS

Signal	Pin	Resistor	Value	Label
8,9,14,16 DGPU_PWROK		R398	4/SEC	GPXD1
38 DGPU_PR_EN		R405	4/SEC	DGPU_PR_EN_E

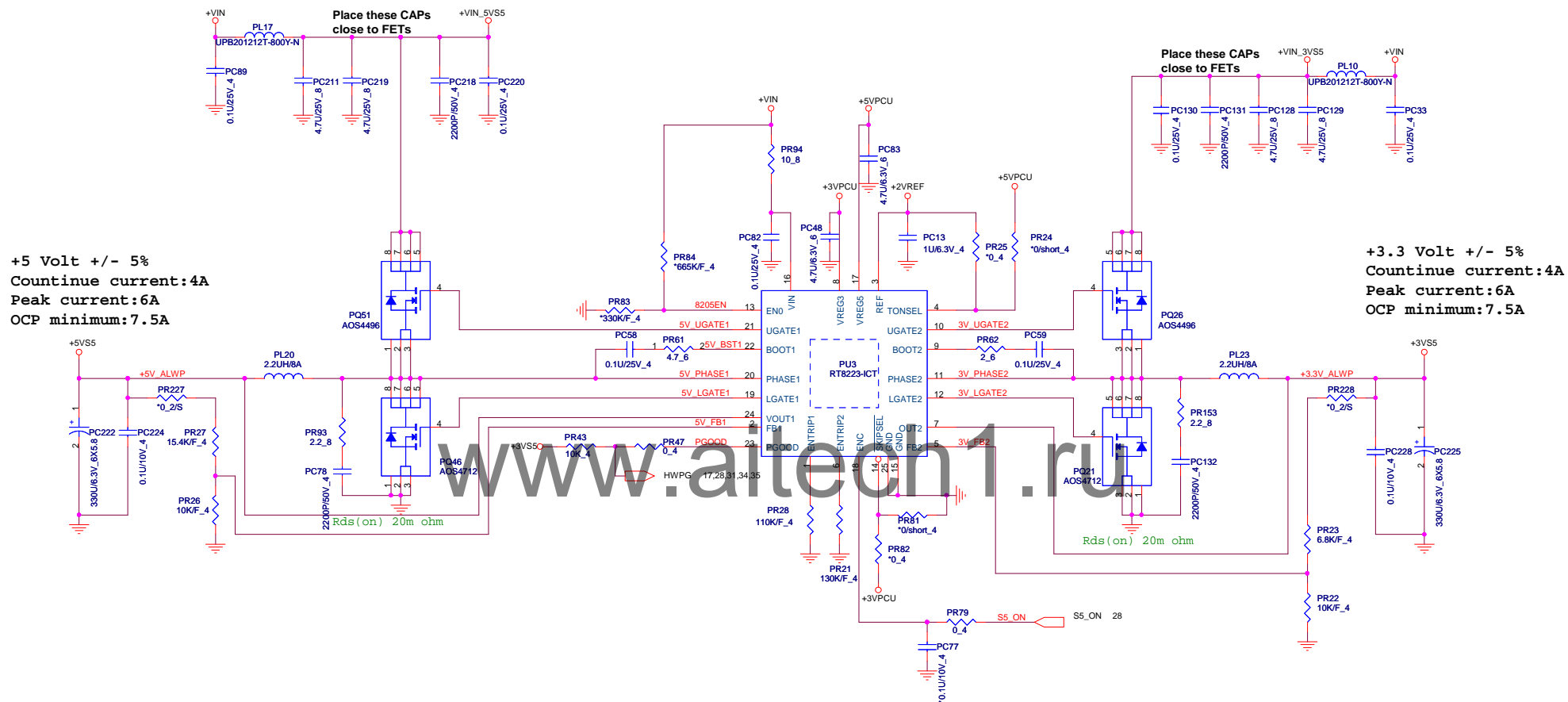


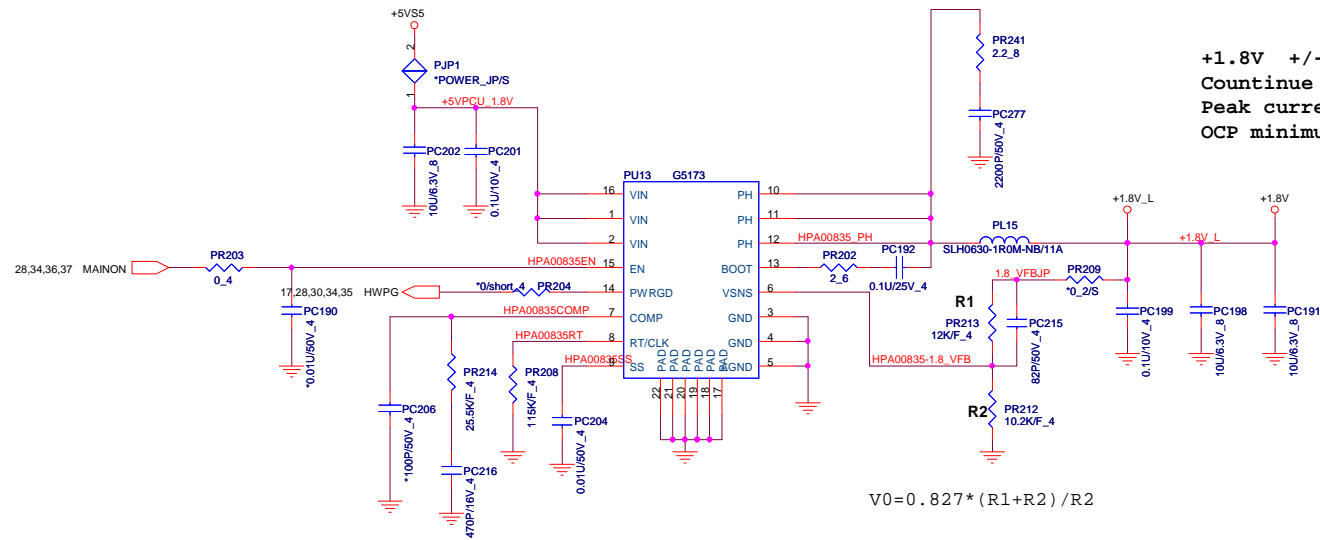
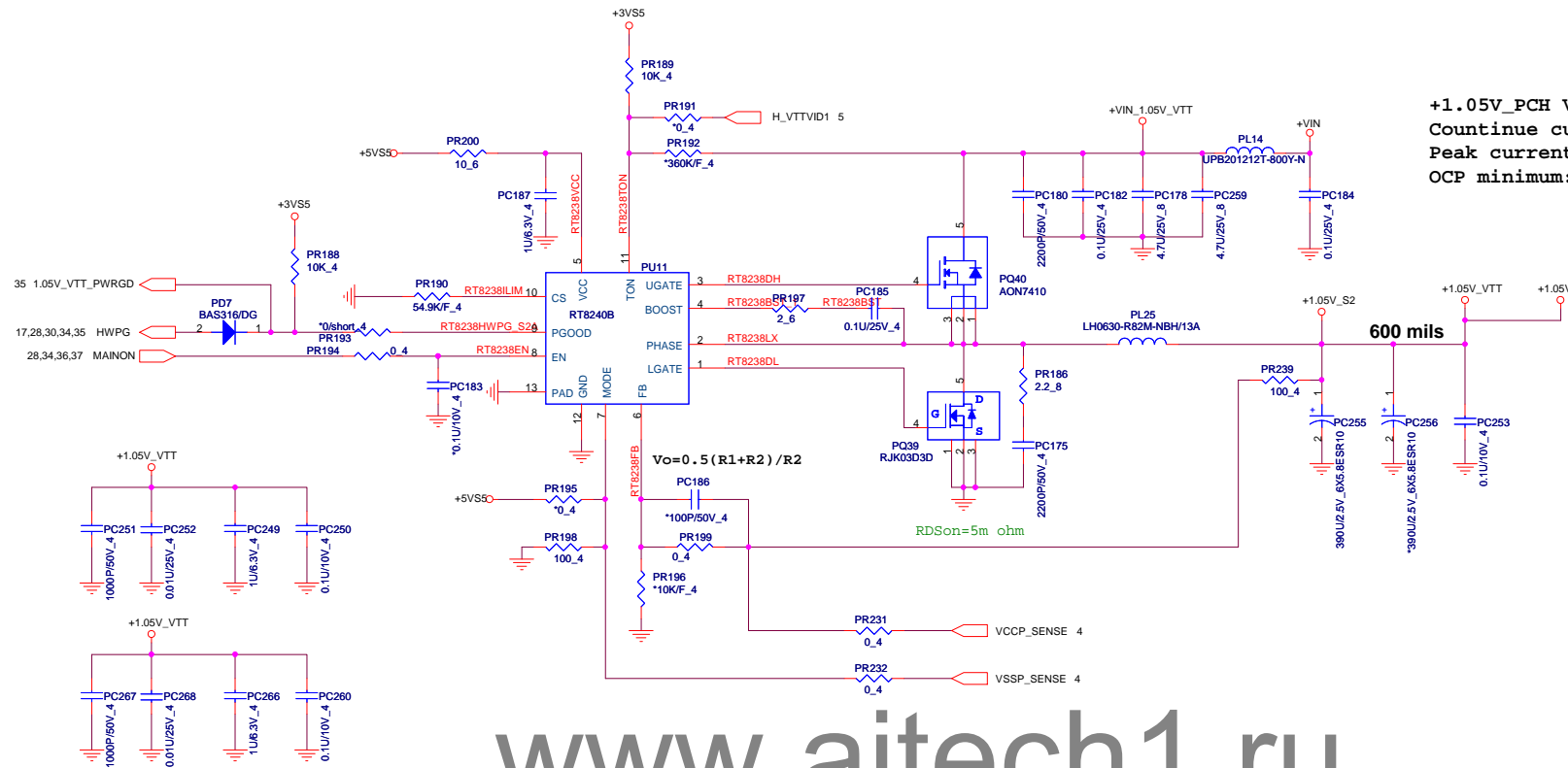
Mini PCI-E Card 1 WLAN

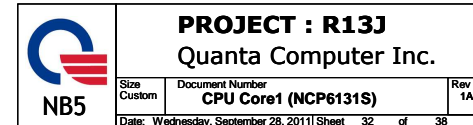
29

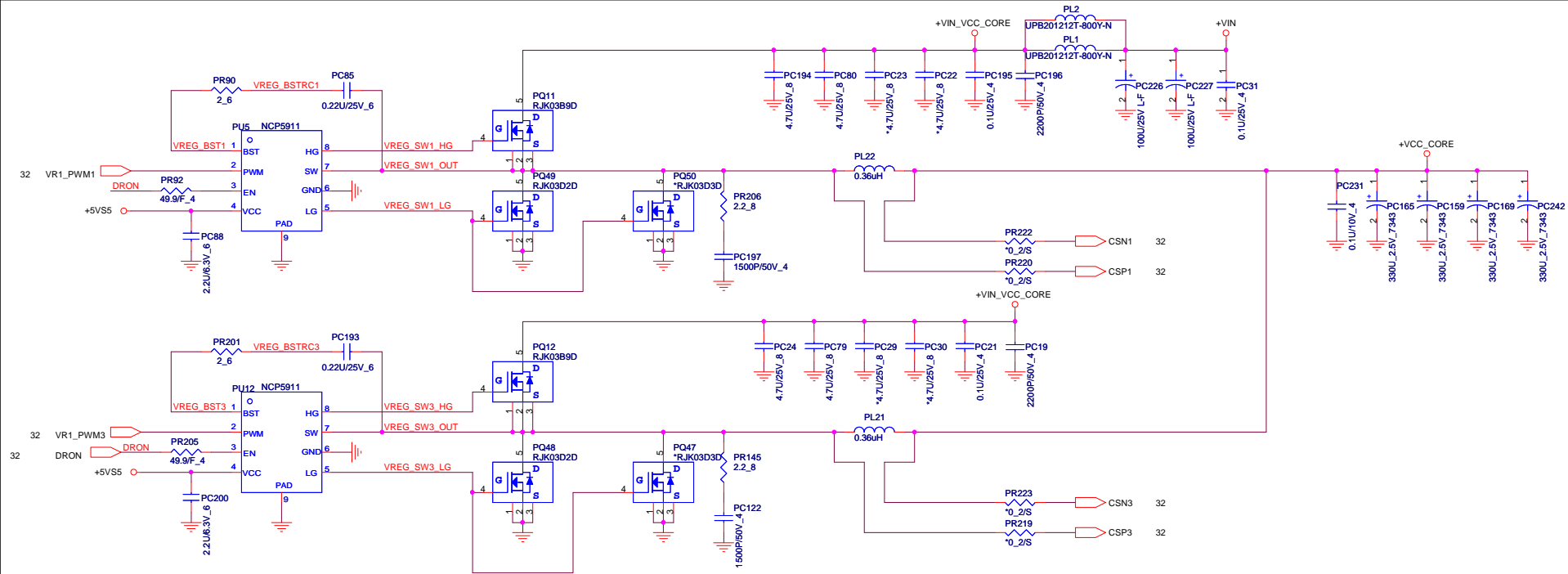


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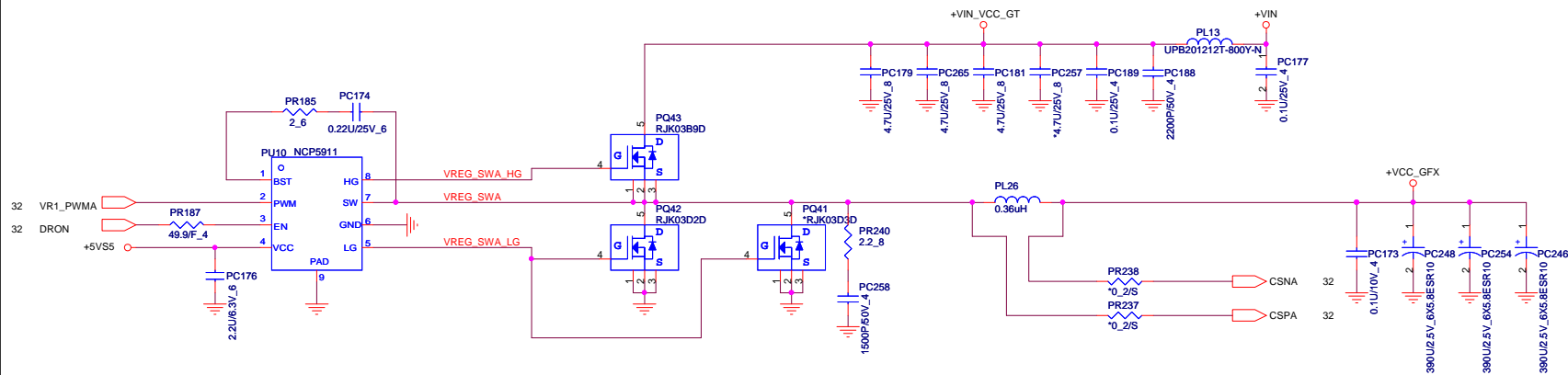








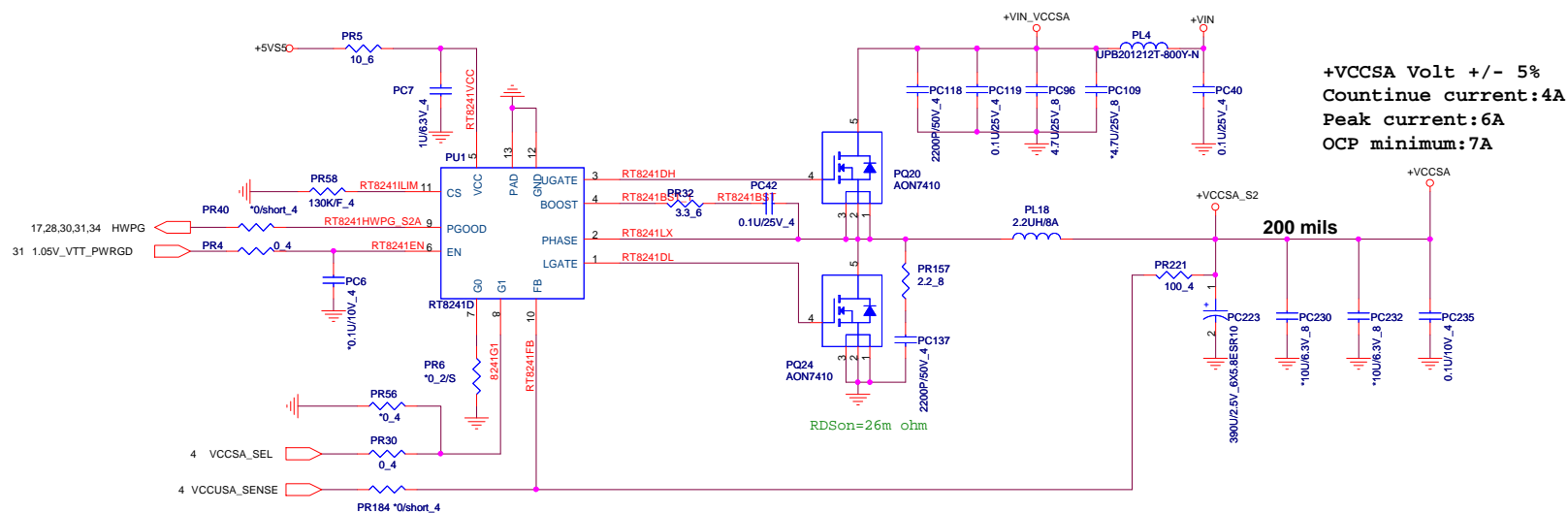
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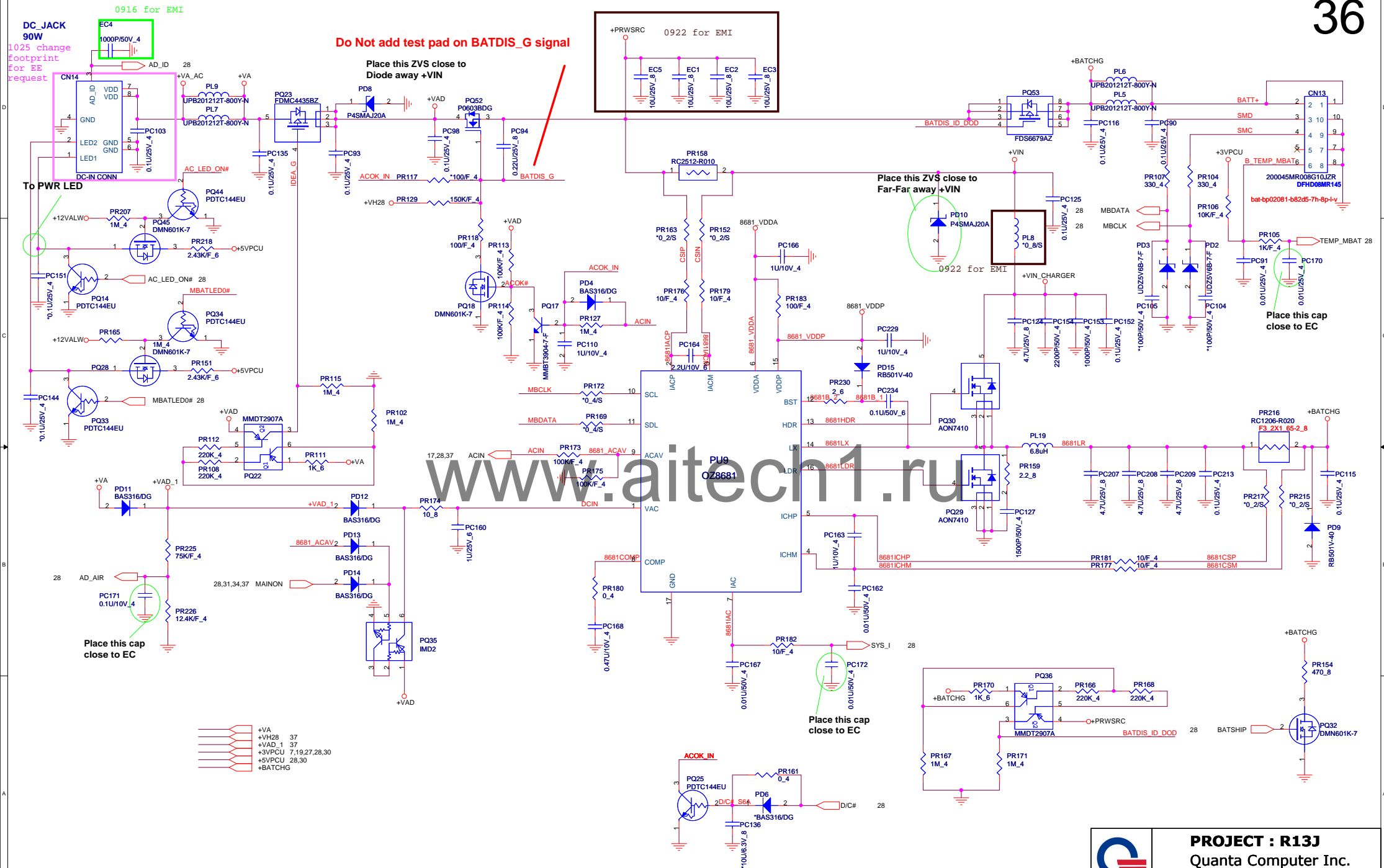
PROJECT : R13J
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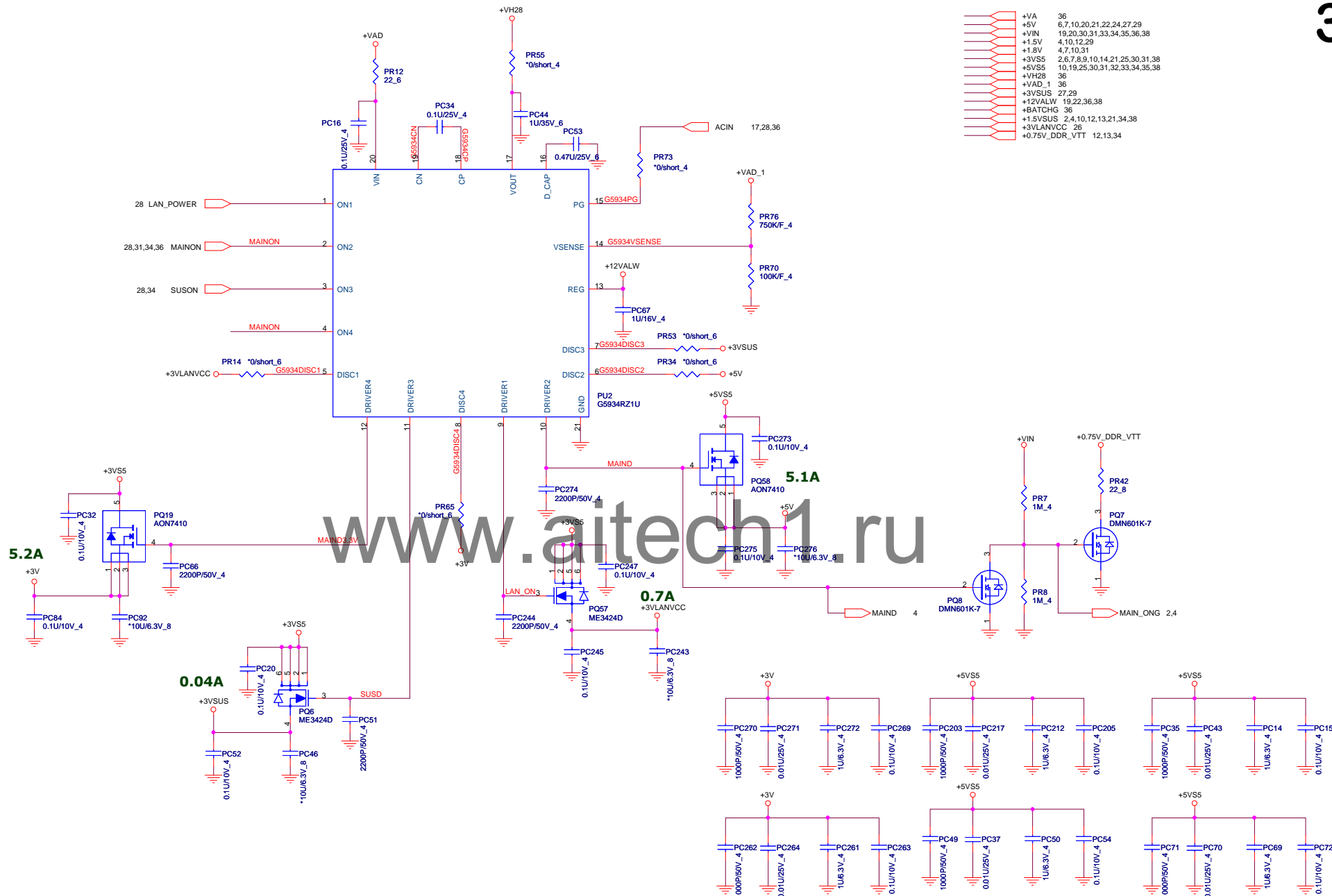
Size Custom	Document Number CPU Core2 (NCP5911)	Rev 1A
Date: Wednesday, September 28, 2011 Sheet 33 of 38		

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38

